36 V, 1 A, Synchronous, Step-Down, DC-to-DC Regulator with External Clock Synchronization

Data Sheet **ADP2442**

FEATURES

- Wide input voltage range from 4.5 V to 36 V
- Low minimum on time of 50 ns typical
- Maximum load current of 1 A
- High efficiency of up to 94%
- Adjustable output down to 0.6 V
- ±1% output voltage accuracy
- Adjustable switching frequency from 300 kHz to 1 MHz
- External synchronization from 300 kHz to 1 MHz
- Pulse skip mode or forced fixed frequency mode
- Precision enable input pin (EN)
- Open-drain power good
- Internal soft start
- Overcurrent-limit protection
- Shutdown current of less than 15 µA
- UVLO and thermal shutdown
- 12-lead, 3 mm × 3 mm LFCSP package
- Supported by the ADIsimPower™ tool set

APPLICATIONS

- Point of load applications
- Distributed power systems
- Industrial control supplies
- Standard rail conversion to 24 V/12 V/5 V/3.3 V

TYPICAL CIRCUIT CONFIGURATION

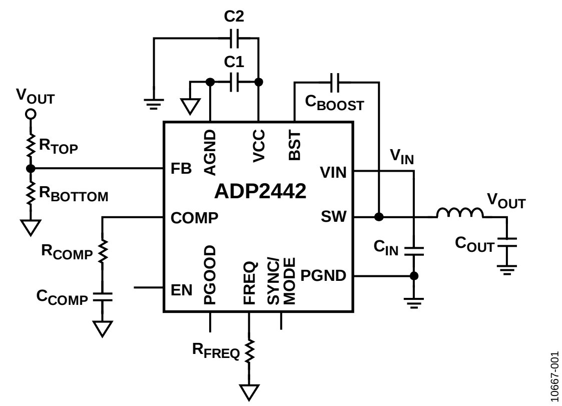

Figure 1.

GENERAL DESCRIPTION

The ADP2442 is a constant frequency, current mode control, synchronous, step-down, dc-to-dc regulator that is capable of driving loads of up to 1 A with excellent line and load regulation characteristics. The ADP2442 operates with a wide input voltage range from 4.5 V to 36 V, which makes it ideal for regulating power from a wide variety of sources. In addition, the ADP2442 has very low minimum on time (50 ns) and is, therefore, suitable for applications requiring a very high step-down ratio.

The output voltage can be adjusted from 0.6 V to 0.9 × V_{IN}. High efficiency is obtained with integrated low resistance N-channel MOSFETs for both high-side and low-side devices.

The switching frequency is adjustable from 300 kHz to 1 MHz with an external resistor. The ADP2442 also has an accurate power-good (PGOOD) open-drain output signal.

The ADP2442 offers the flexibility of external clock synchronization. The switching frequency can be synchronized to an external clock, applied to the SYNC/MODE pin. The ADP2442 can also be configured to operate in the forced fixed frequency mode for low EMI or power saving mode to reduce the switching losses at light load.

The ADP2442 uses hiccup mode to protect the IC from short circuits or from overcurrent conditions on the output. The internal soft start limits inrush current during startup for a wide variety of load capacitances. Other key features include input undervoltage lockout (UVLO), thermal shutdown (TSD), and precision enable (EN), which can also be used as a logic level shutdown input.

The ADP2442 is available in a 3 mm × 3 mm, 12-lead LFCSP package and is rated for a junction temperature range from −40°C to +125°C.

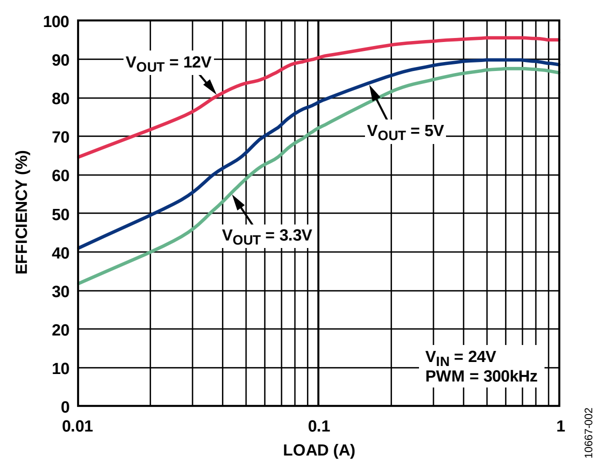

Figure 2. Efficiency vs. Load Current, V_{IN} = 24 V

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REVISION HISTORY

11/12—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 4.5 V to 36 V, T_J = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY						
Input Voltage Range	V_{IN}		4.5		36	V
Supply Current	I_{VIN}	V_{EN} = 1.5 V not switching		1.7	2	mA
Shutdown Current	I_{SHDN}	V_{EN} = AGND		10	15	µA
UVLO						
Threshold	V_{UVLO}	V_{IN} falling	3.8	4	4.2	V
Hysteresis				200		mV
INTERNAL REGULATOR						
Regulator Output Voltage	V_{CC}	V_{IN} = 5 V to 36 V		5	5.5	V
OUTPUT						
Output Voltage Range	V_{OUT}		0.6		0.9 × V_{IN}	V
Maximum Output Current	I_{OUT}		1			A
Feedback Regulation Voltage	V_{FB}	T_J = −40°C to +85°C	0.594	0.6	0.606	V
		T_J = −40°C to +125°C	0.591	0.6	0.609	V
Line Regulation				0.005		%/V
Load Regulation				0.05		%/A
ERROR AMPLIFIER						
Feedback Bias Current	I_{FB_BIAS}	V_{FB} = 0.6 V		50	200	nA
Transconductance	g_m	I_{COMP} = ±20 µA	200	250	300	µA/V
Open-Loop Voltage Gain[1]	A_{VOL}			65		dB
MOSFETS						
High-Side Switch On Resistance[2]	$R_{DS\_H(ON)}$	BST – SW = 5 V		170	270	mΩ
Low-Side Switch On Resistance[2]	$R_{DS\_L(ON)}$	V_{CC} = 5 V		120	180	mΩ
Leakage Current	I_{LKG}	V_{EN} = AGND		1	25	µA
Minimum On Time[3]	t_{ON_MIN}	All switching frequencies		50	65	ns
Minimum Off Time[4]	t_{OFF_MIN}			165	175	ns
CURRENT SENSE						
Current Sense Amplifier Gain	G_{CS}		1.6	2	2.4	A/V
Hiccup Time		f_{SW} = 300 kHz to1 MHz		6		ms
Number of Cumulative Current-Limit Cycles to Enter Hiccup Mode				8		Events
Peak Current Limit	I_{CL}		1.4	1.6	1.8	A
FREQUENCY						
Switching Frequency Range	f_{SW}		300		1000	kHz
Frequency Set Accuracy		FREQ pin = 308 kΩ	270	300	330	kHz
		FREQ pin = 92.5 kΩ	900	1000	1100	kHz
Frequency Synchronization Range			300		1000	kHz
SOFT START						
Soft Start Time	t_{SS}			2		ms
PRECISION ENABLE						
Input Threshold	$V_{EN(RISING)}$		1.15	1.20	1.25	V
Hysteresis	$V_{EN(HYST)}$			100		mV
Leakage Current	I_{IEN_LEAK}	$V_{IN} = V_{EN}$		0.1	1	µA
Thermal Shutdown						
Rising	T_{SD}			150		°C
Hysteresis	$T_{SD(HYST)}$			25		°C

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER GOOD						
PGOOD High, FB Rising Threshold[5]			89	92	95	%
PGOOD Low, FB Rising Threshold[5]			111	115	118	%
PGOOD High, FB Falling Threshold[5]			106	109	112	%
PGOOD Low, FB Falling Threshold[5]			83	86	89	%
PGOOD						
Delay	t_{PGOOD}			50		µs
High Leakage Current	$I_{PGOOD(SRC)}$	$V_{PGOOD} = V_{CC}$		1	10	µA
Pull-Down Resistor	$I_{PGOOD(SNK)}$	FB = 0 V		0.5	0.7	kΩ
SYNC/MODE						
SYNC/MODE Input						
Logic High			2			V
Logic Low					0.8	V
Pulse Width			100			ns

[1] Guaranteed by design.
[2] Measured between VIN and SW pins and includes bond wires and pin resistance.
[3] Based on bench characterization. Measured with V_{IN} = 12 V, V_{OUT} = 1.2 V, load = 1 A, f_{SW} = 1 MHz, and the output in regulation. Measurement does not include dead time.
[4] Based on bench characterization. Measured with V_{IN} = 15 V, V_{OUT} = 12 V, load = 1 A, f_{SW} = 600 kHz, and the output in regulation. Measurement does not include dead time.
[5] This threshold is expressed as a percentage of the nominal output voltage.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN to PGND	−0.3 V to +40 V
EN to AGND	−0.3 V to +40 V
SW to PGND	−0.3 V to +40 V
BST to PGND	−0.3 V to +45 V
VCC to AGND	−0.3 V to +6 V
BST to SW	−0.3 V to +6 V
FREQ, PGOOD, SYNC/MODE, COMP, FB to AGND	−0.3 V to +6 V
PGND to AGND	±0.3 V
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages based on a 4-layer standard JEDEC board.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
12-Lead LFCSP	40	2.4	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

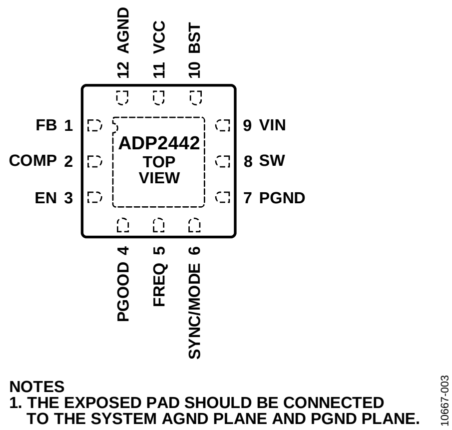

Figure 3. Pin Configuration, Top View

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	FB	Feedback. The FB regulation voltage is 0.6 V. Connect this pin to a resistor divider from the output of the dc-to-dc regulator.
2	COMP	Error Amplifier Compensation. Connect a resistor and a capacitor in series to ground.
3	EN	Precision Enable. This features offers ±5% accuracy when using a 1.25 V reference voltage. Pull this pin high to enable the regulator and pull it low to disable the regulator. Do not leave this pin floating.
4	PGOOD	Active High Power Good Output. This pin is pulled low when the output is out of regulation.
5	FREQ	Switching Frequency. A resistor to AGND sets the switching frequency (see the Setting the Switching Frequency section). Do not leave this pin floating.
6	SYNC/MODE	External Clock Synchronization/Mode Pin. This pin can be used for external frequency synchronization and for setting forced fixed frequency mode or pulse skip mode. SYNC/MODE accepts an external clock signal, and when pulled high to 5 V, it sets the mode as forced fixed frequency mode. When this pin is tied to AGND, pulse skip mode is enabled. Do not leave the SYNC/MODE pin floating.
7	PGND	Power Ground. Connect a decoupling ceramic capacitor as close as possible between the VIN pin and PGND. Connect this pin directly to the exposed pad.
8	SW	Switch. The midpoint for the drain of the low-side N-channel power MOSFET switch and the source for the high-side N-channel power MOSFET switch.
9	VIN	Power Supply Input. Connect this pin to the input power source, and connect a bypass ceramic capacitor directly from this pin to PGND, as close as possible to the IC. The operation voltage is 4.5 V to 36 V.
10	BST	Boost. Connect a 10 nF ceramic capacitor between the BST and SW pins as close to the IC as possible to form a floating supply for the high-side N-channel power MOSFET driver. This capacitor is required to drive the gate of the N-channel power MOSFET above the supply voltage.
11	VCC	Output of the Internal Low Dropout Regulator. This pin supplies power for the internal controller and driver circuitry. Connect a 1 µF ceramic capacitor between VCC and AGND and a 1 µ F ceramic capacitor between VCC and PGND. The VCC output is active when the EN pin voltage is more than 0.7 V.
12	AGND	Analog Ground. This pin is the internal ground for the control functions. Connect this pin to the exposed pad.
	EP	Exposed Pad. Connect the exposed pad to the system AGND plane and PGND plane.

TYPICAL PERFORMANCE CHARACTERISTICS

EFFICIENCY IN FORCED FIXED FREQUENCY MODE

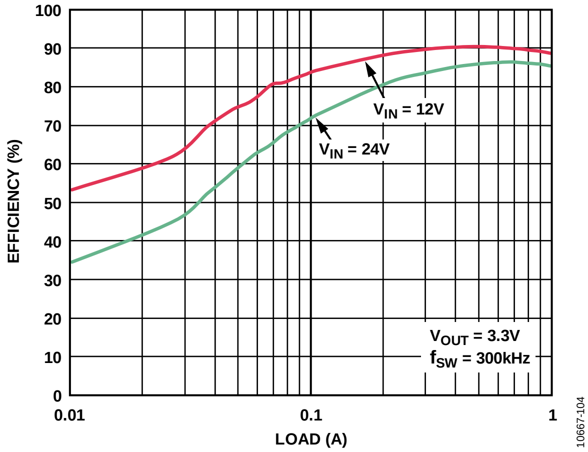

Figure 4. Efficiency vs. Load Current, V_{OUT} = 3.3 V, f_{SW} = 300 kHz

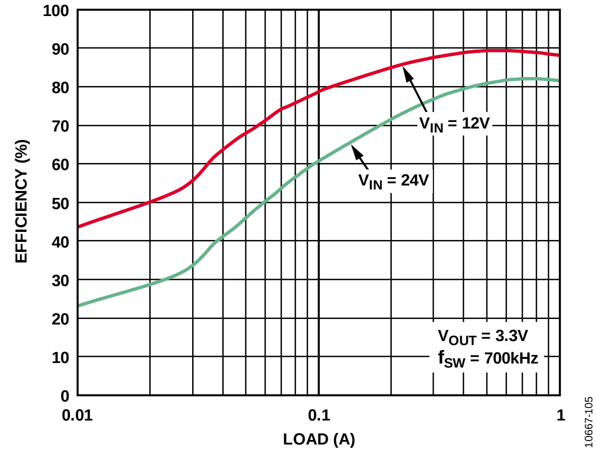

Figure 7. Efficiency vs. Load Current, V_{OUT} = 3.3 V, f_{SW} = 700 kHz

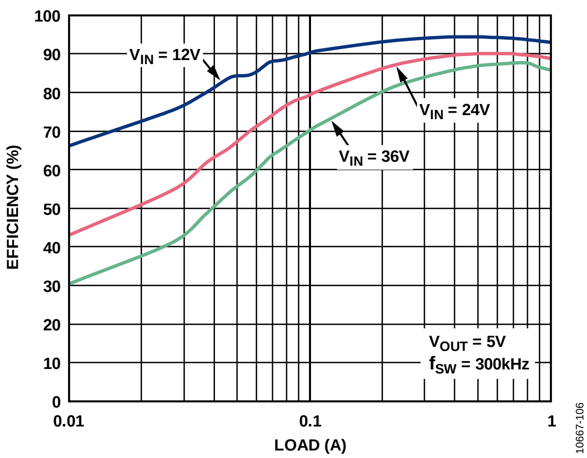

Figure 5. Efficiency vs. Load Current, V_{OUT} = 5 V, f_{SW} = 300 kHz

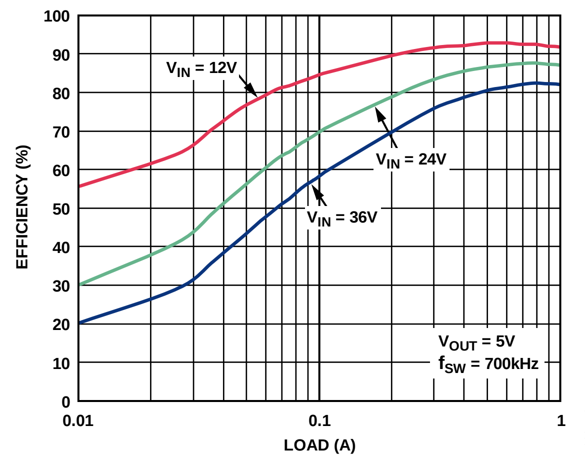

Figure 8. Efficiency vs. Load Current, V_{OUT} = 5 V, f_{SW} = 700 kHz

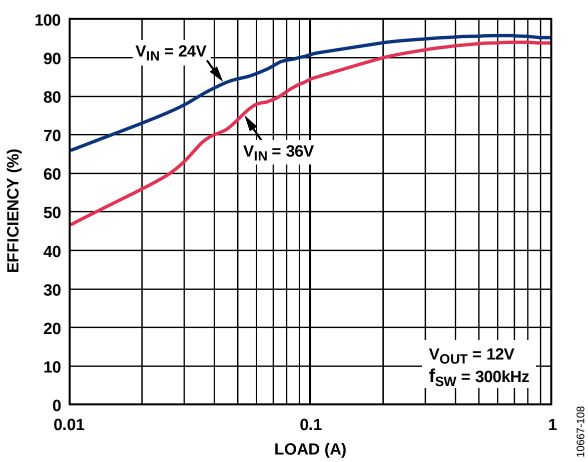

Figure 6. Efficiency vs. Load Current, V_{OUT} = 12 V, f_{SW} = 300 kHz

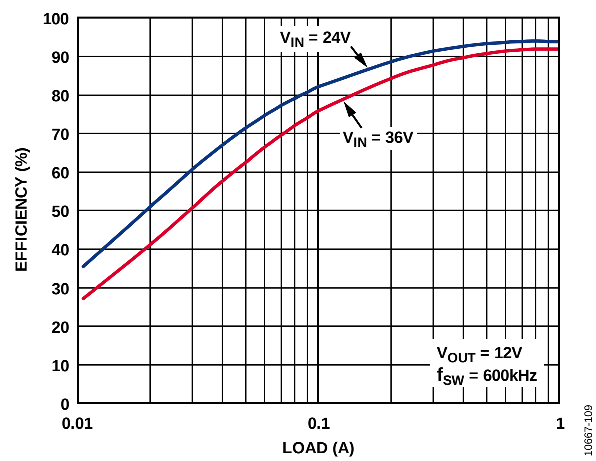

Figure 9. Efficiency vs. Load Current, V_{OUT} = 12 V, f_{SW} = 600 kHz

EFFICIENCY IN PULSE SKIP MODE

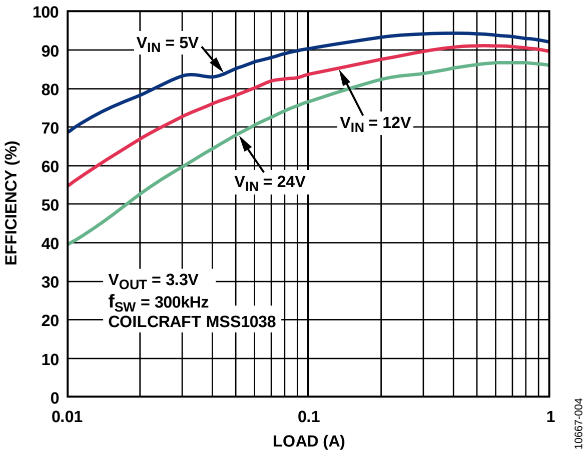

Figure 10. Efficiency vs. Load Current, V_{OUT} = 3.3 V, f_{SW} = 300 kHz

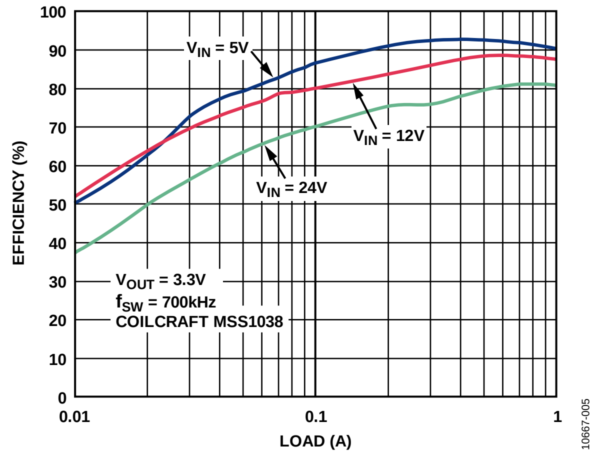

Figure 13. Efficiency vs. Load Current, V_{OUT} = 3.3 V, f_{SW} = 700 kHz

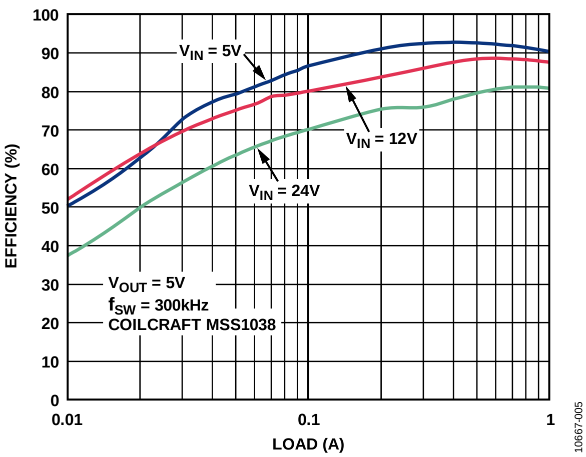

Figure 11. Efficiency vs. Load Current, V_{OUT} = 5 V, f_{SW} = 300 kHz

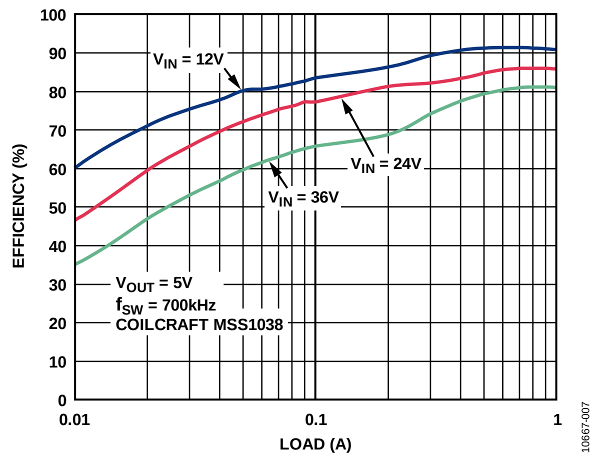

Figure 14. Efficiency vs. Load Current, V_{OUT} = 5 V, f_{SW} = 700 kHz

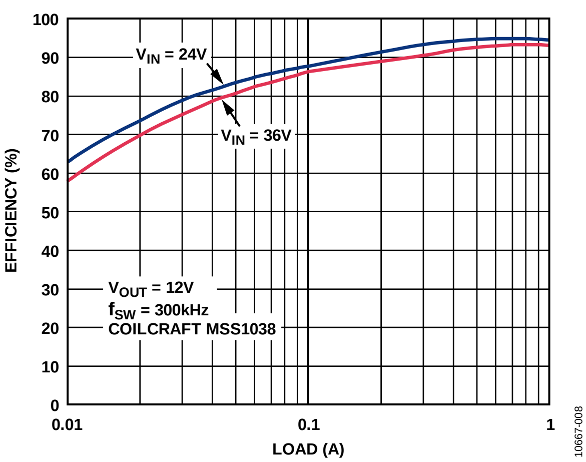

Figure 12. Efficiency vs. Load Current, V_{OUT} = 12 V, f_{SW} = 300 kHz

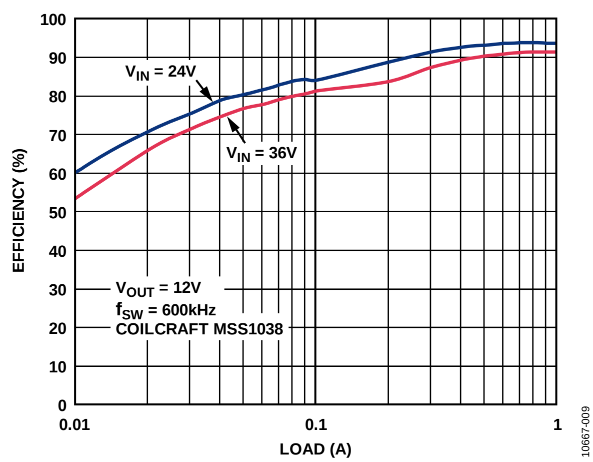

Figure 15. Efficiency vs. Load Current, V_{OUT} = 12 V, f_{SW} = 600 kHz

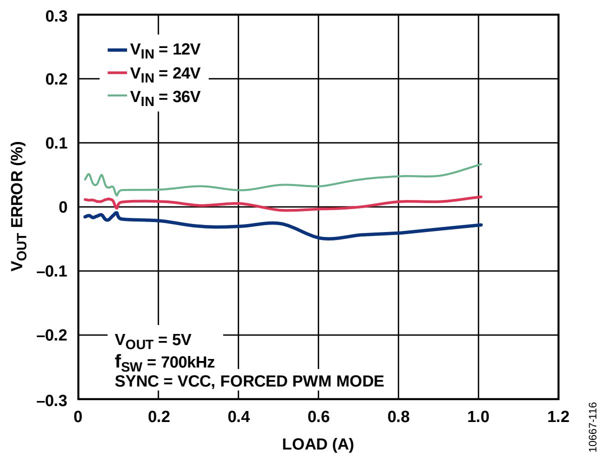

Figure 16. Load Regulation for Different Supplies

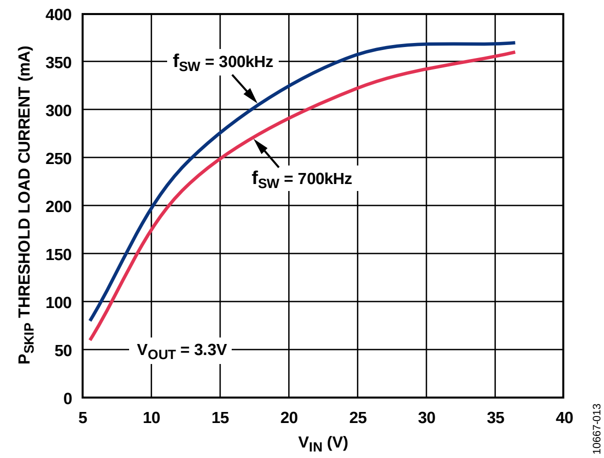

Figure 19. Pulse Skip (P_{SKIP}) Threshold Load Current, V_{OUT} = 3.3 V

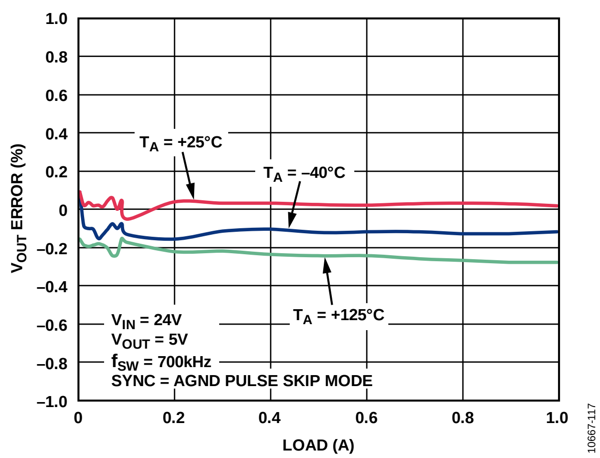

Figure 17. Load Regulation for Different Temperatures

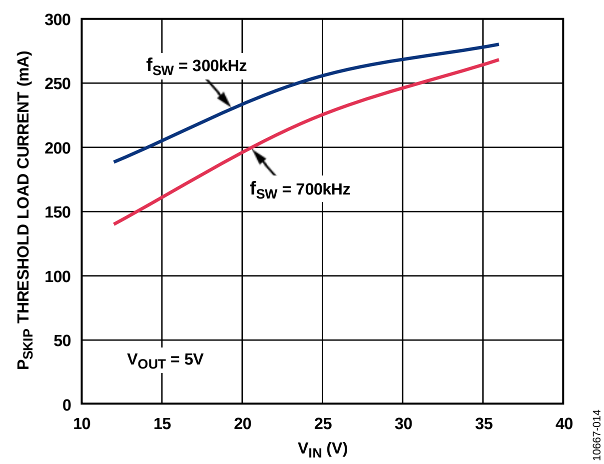

Figure 20. Pulse Skip Threshold Load Current, V_{OUT} = 5 V

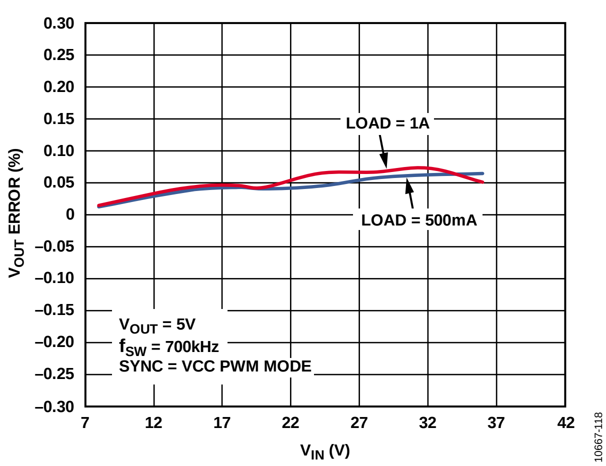

Figure 18. Line Regulation, V_{OUT} = 5 V for Different Loads

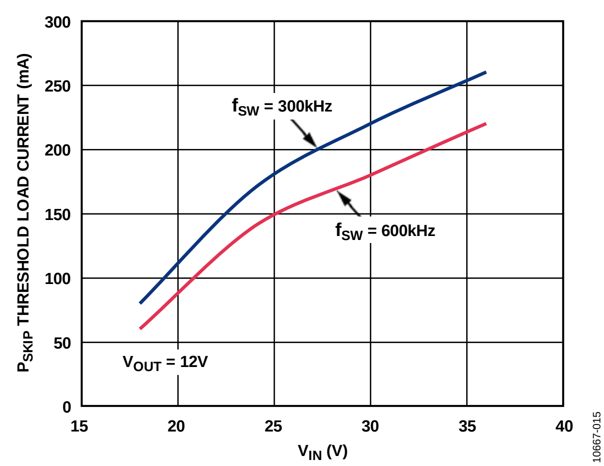

Figure 21. Pulse Skip Threshold Load Current, V_{OUT} = 12 V

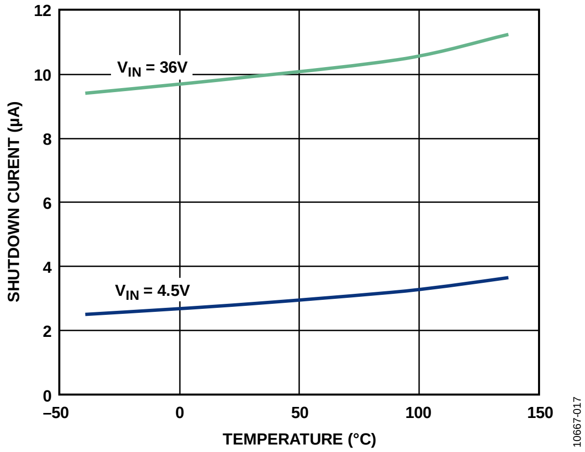

Figure 22. Shutdown Current vs. Temperature

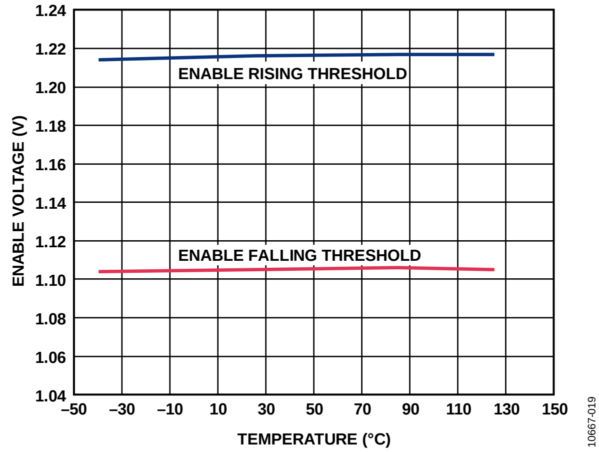

Figure 25. Enable Threshold vs. Temperature

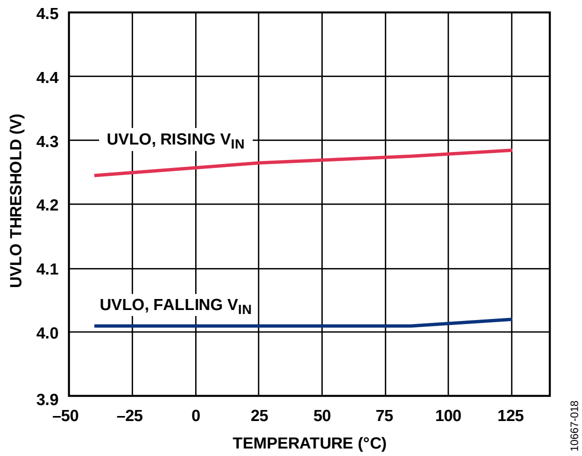

Figure 23. UVLO Threshold vs. Temperature

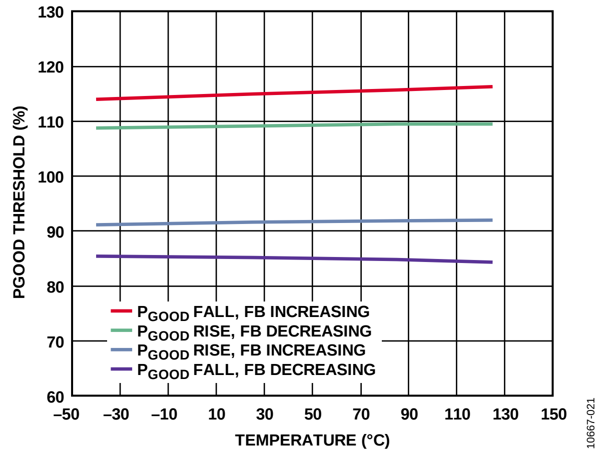

Figure 26. PGOOD Threshold vs. Temperature

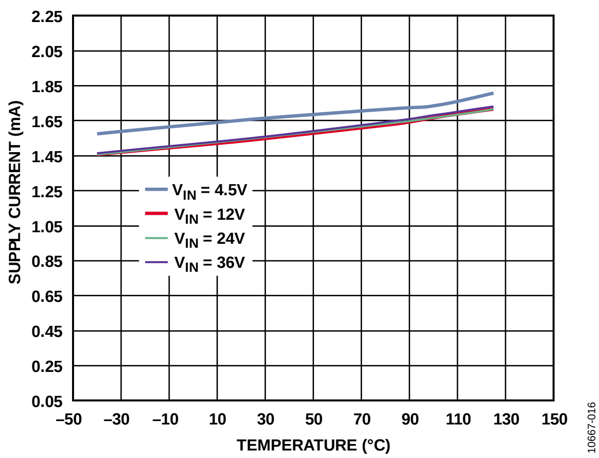

Figure 24. Supply Current vs. Temperature

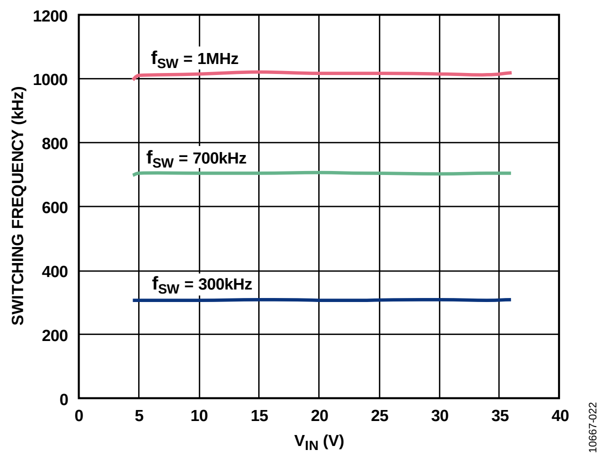

Figure 27. Switching Frequency vs. Supply

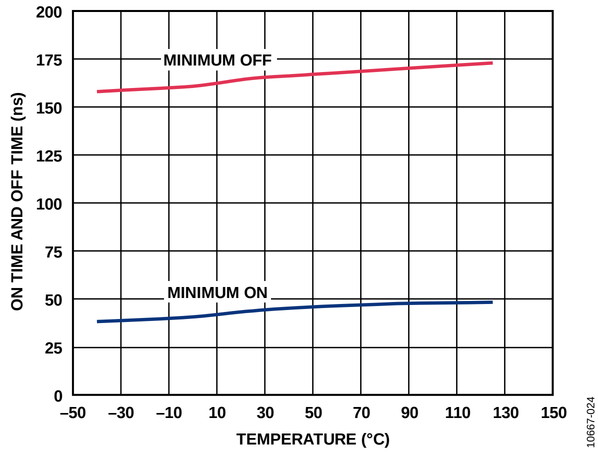

Figure 28. Minimum On Time and Minimum Off Time vs. Temperature

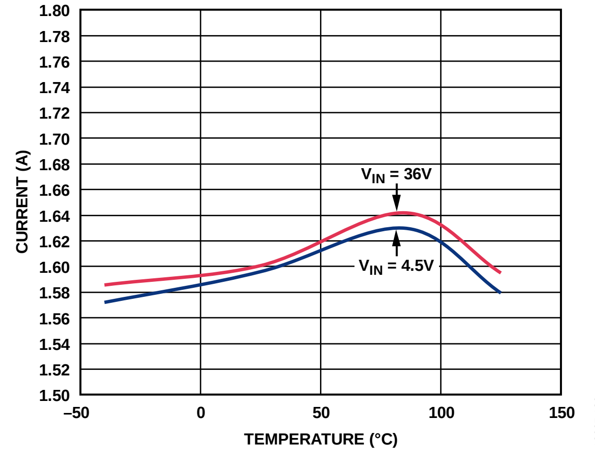

Figure 31. Current Limit vs. Temperature

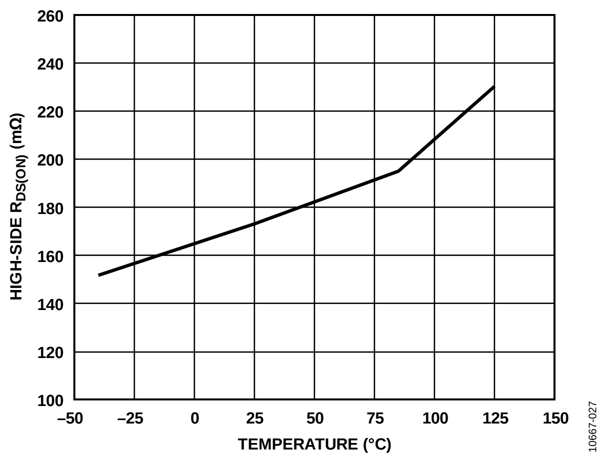

Figure 29. High-Side $R_{DS(ON)}$ vs. Temperature

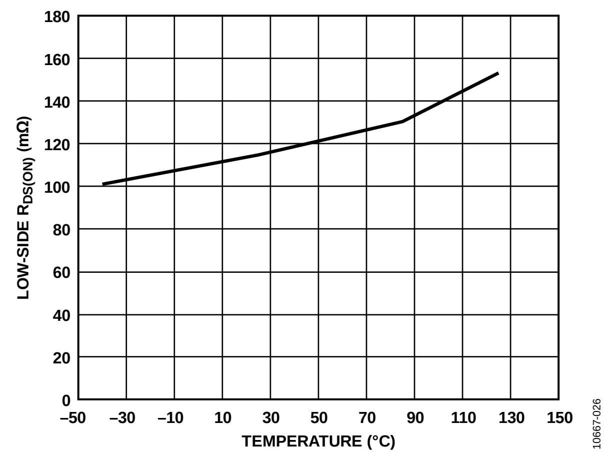

Figure 32. Low-Side $R_{DS(ON)}$ vs. Temperature

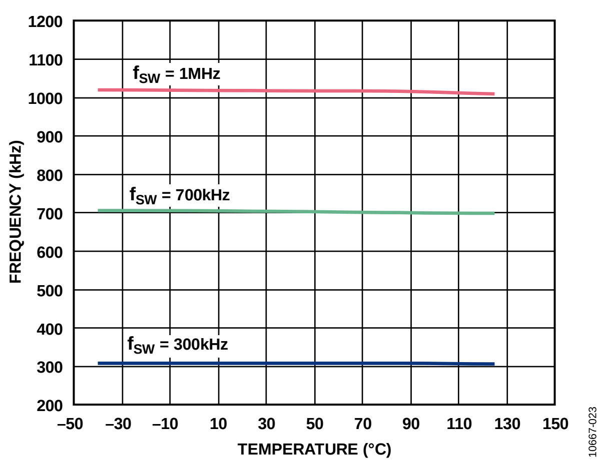

Figure 30. Switching Frequency vs. Temperature

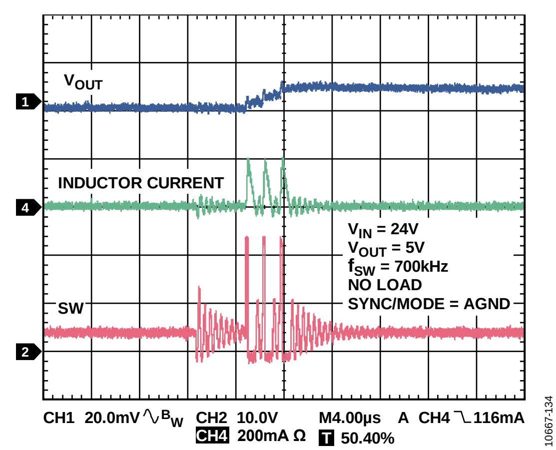

Figure 33. Pulse Skip Mode, V_{IN} = 24 V, V_{OUT} = 5 V, f_{SW} = 700 kHz, No Load, SYNC/MODE = AGND

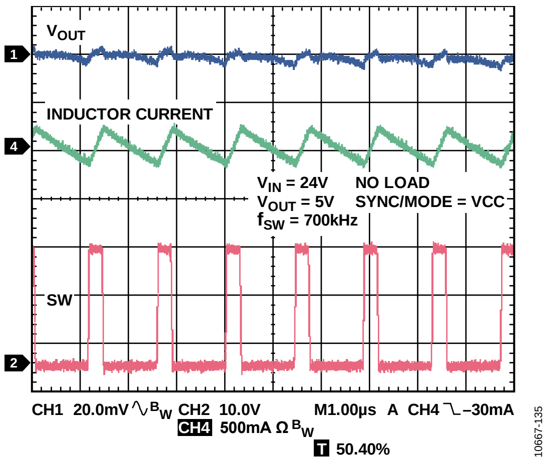

Figure 34. PWM Mode
V_{IN} = 24 V, V_{OUT} = 5 V, f_{SW} = 700 kHz, Load = No Load, SYNC/MODE = VCC

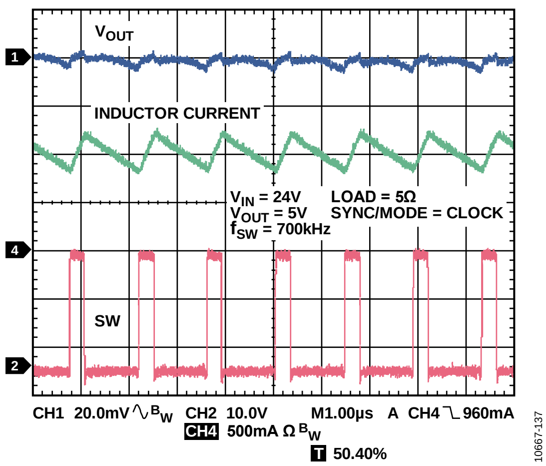

Figure 35. PWM Mode with External Clock, V_{IN} = 24 V, V_{OUT} = 5 V, f_{SW} = 700 kHz, Load = 5 Ω, SYNC/MODE = Clock

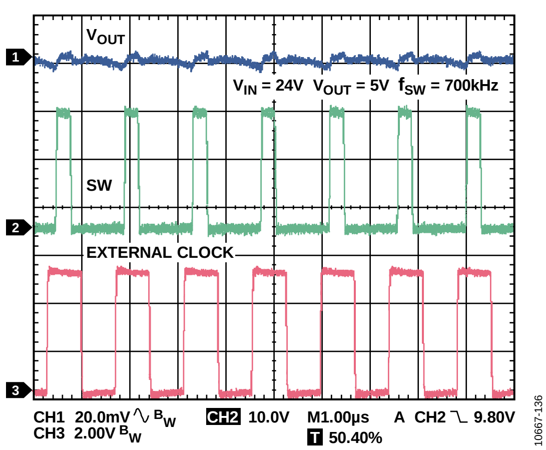

Figure 36. External Clock Synchronization,
V_{IN} = 24 V, V_{OUT} = 5 V, f_{SW} = 700 kHz, SYNC/MODE = Clock

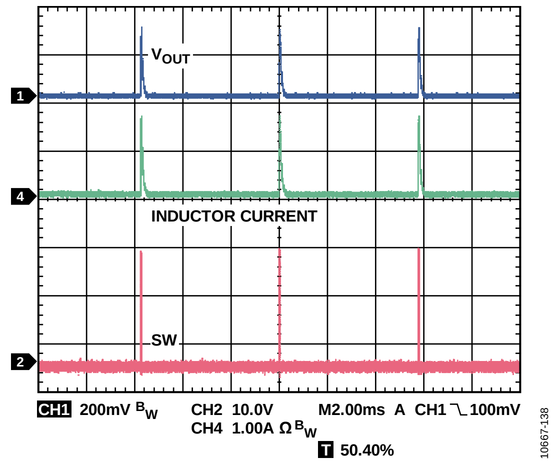

Figure 37. Hiccup Mode, V_{IN} = 24 V, V_{OUT} = 5 V, f_{SW} = 700 kHz, Output Shorted to PGND

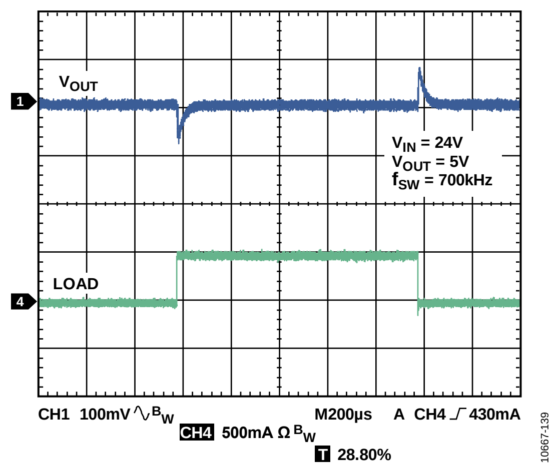

Figure 38. Load Transient Response, V_{IN} = 24 V, V_{OUT} = 5 V, f_{SW} = 700 kHz, SYNC/MODE = Clock, Load Step = 500 mA

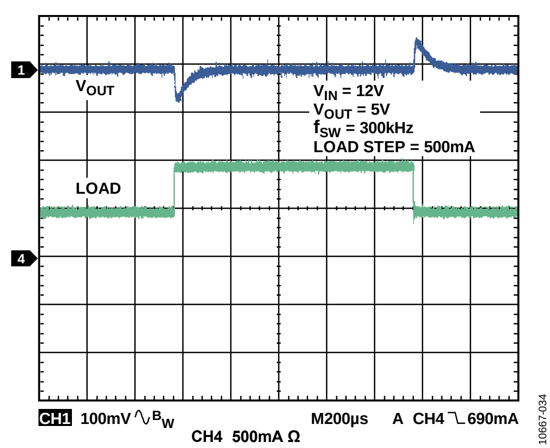

Figure 39. Load Transient Response,
V_{IN} = 12 V, V_{OUT} = 5 V, f_{SW} = 300 kHz, Load Step = 500 mA

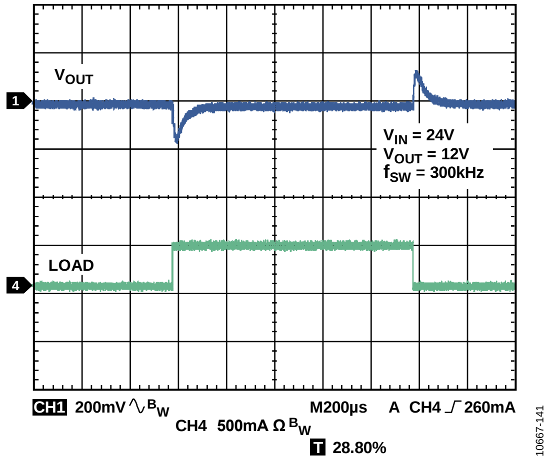

Figure 40. Load Transient Response, V_{IN} = 24 V, V_{OUT} = 12 V, f_{SW} = 300 kHz, SYNC/MODE = Clock, Load Step = 500 mA

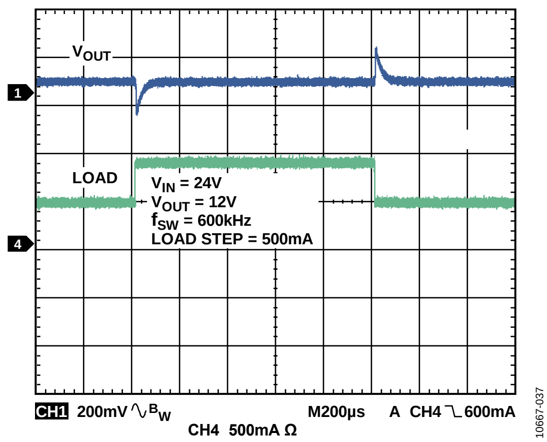

Figure 41. Load Transient Response, V_{IN} = 24 V, V_{OUT} = 12 V, f_{SW} = 600 kHz, Load Step = 500 mA

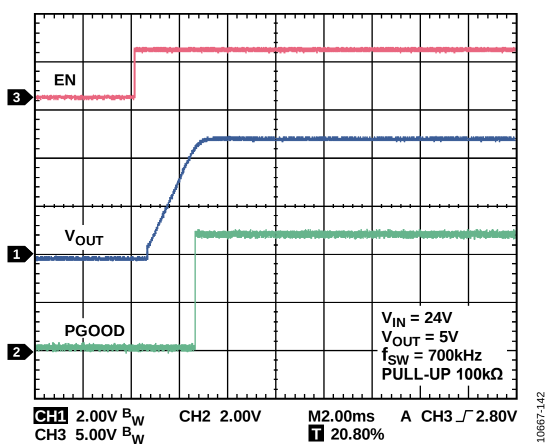

Figure 42. Power-Good Startup, V_{IN} = 24 V, V_{OUT} = 5 V, f_{SW} = 700 kHz

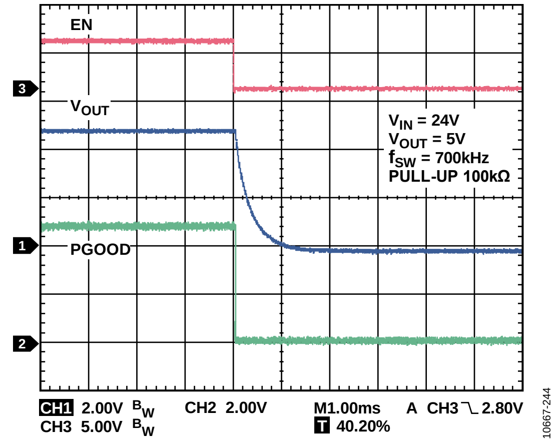

Figure 43. Power-Good Shutdown, V_{IN} = 24 V, V_{OUT} = 5 V, f_{SW} = 700 kHz

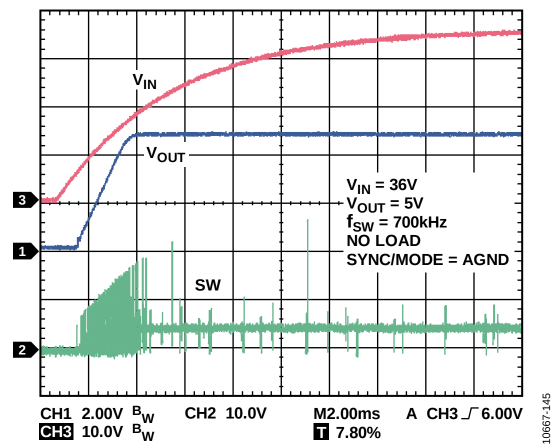

Figure 44. Startup with V_{IN}, Pulse Skip Mode, V_{IN} = 36 V, V_{OUT} = 5 V, f_{SW} = 700 kHz, No Load, SYNC/MODE = AGND

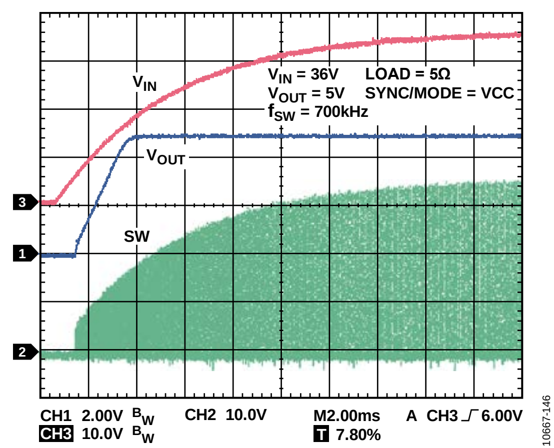

Figure 45. Startup with V_{IN}, PWM Mode, V_{IN} = 36 V, V_{OUT} = 5 V, f_{SW} = 700 kHz, Load = 5 Ω, SYNC/MODE = VCC

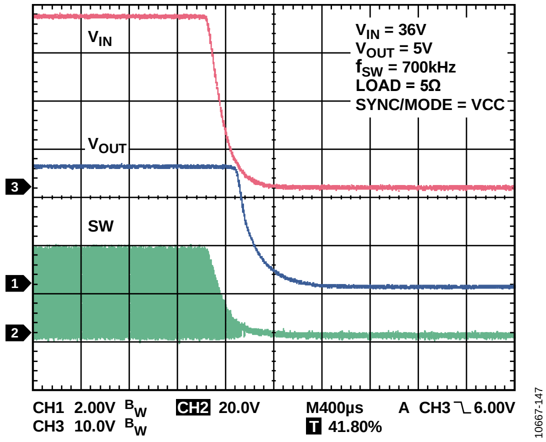

Figure 46. Shutdown with V_{IN}, PWM Mode, V_{IN} = 36 V, V_{OUT} = 5 V, f_{SW} = 700 kHz, Load = 5 Ω, SYNC/MODE = VCC

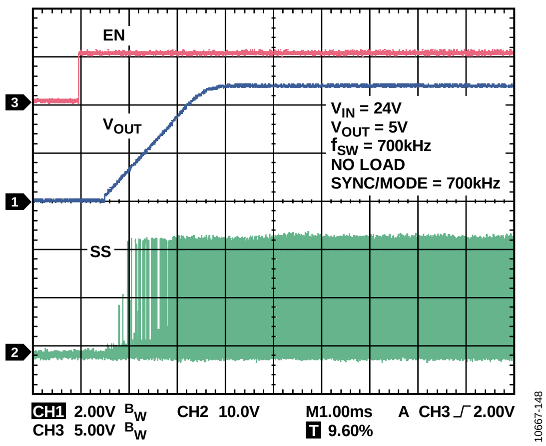

Figure 47. Startup with Precision Enable, V_{IN} = 24 V, V_{OUT} = 5 V, f_{SW} = 700 kHz, Load = No Load, SYNC/MODE = 700 kHz

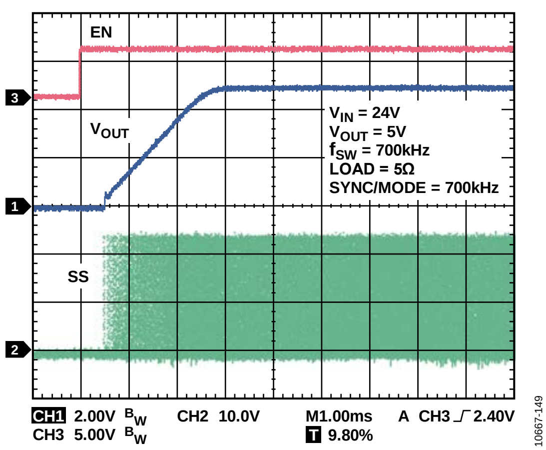

Figure 48. Startup with Precision Enable, V_{IN} = 24 V, V_{OUT} = 5 V, f_{SW} = 700 kHz, Load = 5 Ω, SYNC/MODE = 700 kHz

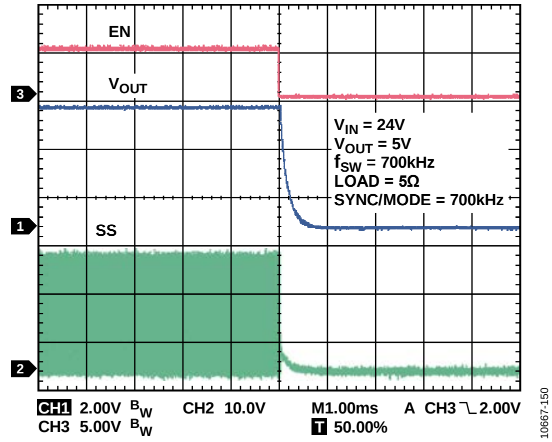

Figure 49. Shutdown with Precision Enable, V_{IN} = 24 V, V_{OUT} = 5 V, f_{SW} = 700 kHz, Load = 5 Ω, SYNC/MODE = 700 kHz

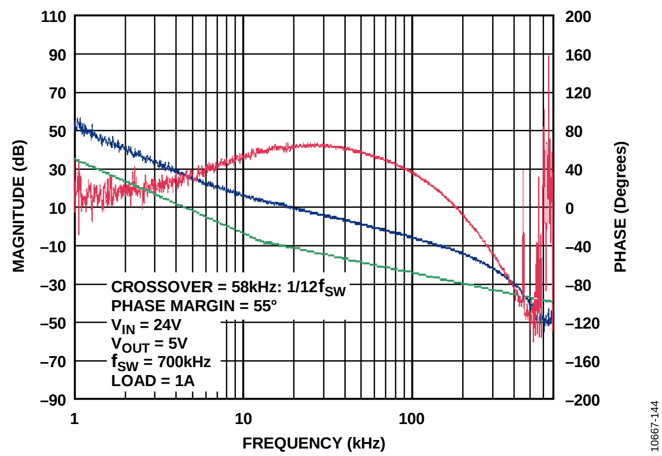

Figure 50. Magnitude and Phase vs. Frequency

INTERNAL BLOCK DIAGRAM

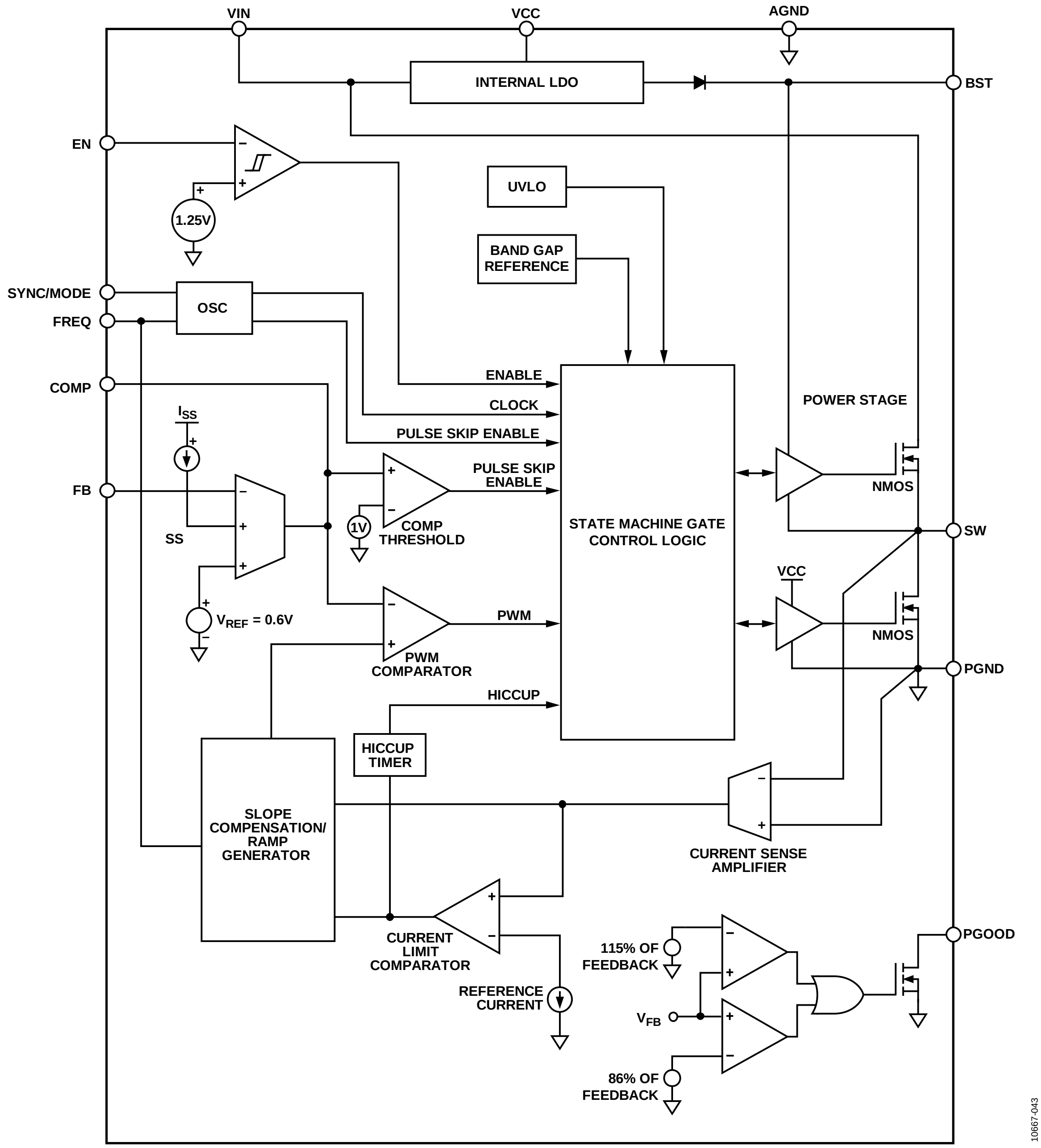

Figure 51. Internal Block Diagram

THEORY OF OPERATION

The ADP2442 is a fixed frequency, current mode control, step-down, synchronous switching regulator that is capable of driving 1 A loads. The device operates with a wide input voltage range from 4.5 V to 36 V, and its output is adjustable from 0.6 V to 0.9 V × V_{IN}. The integrated high-side N-channel power MOSFET and the low-side N-channel power MOSFET yield high efficiency at medium to heavy loads. Pulse skip mode is available to improve efficiency at light loads.

The ADP2442 includes programmable features, such as output voltage, switching frequency, and power good. These features are programmed externally via tiny resistors and capacitors. The ADP2442 also includes protection features, such as UVLO with hysteresis, output short-circuit protection, and thermal shutdown.

CONTROL ARCHITECURE

The ADP2442 is based on an emulated peak current mode control architecture. The ADP2442 can operate in both fixed frequency and pulse skip modes.

Fixed Frequency Mode

A basic block diagram of the control architecture is shown in Figure 52. The ADP2442 can be configured in fixed frequency mode. The output voltage, V_{OUT}, is sensed on the feedback pin, FB. An error amplifier integrates the error between the feedback voltage (V_{FB}) and the reference voltage (V_{REF} = 0.6 V) to generate an error voltage at the COMP pin.

A current sense amplifier senses the valley inductor current (I_L) during the off period when the low-side power MOSFET is on and the high-side power MOSFET is off. An internal oscillator initiates a pulse-width modulation (PWM) pulse to turn off the low-side power MOSFET and turn on the high-side power MOSFET at a fixed switching frequency.

When the high-side N-channel power MOSFET is enabled, the valley inductor current information is added to an emulated ramp signal and the PWM comparator compares this value to the error voltage on the COMP pin. The output of the PWM comparator modulates the duty cycle by adjusting the trailing edge of the PWM pulse that turns off the high-side power MOSFET and turns on the low-side power MOSFET.

Slope compensation is programmed internally into the emulated ramp signal and is automatically selected, depending on the input voltage, output voltage, and switching frequency. This prevents subharmonic oscillations for near or greater than 50% duty cycle operation. The one restriction of this feature is that the inductor ripple current must be set between 0.2 A and 0.5 A to provide sufficient current information to the loop.

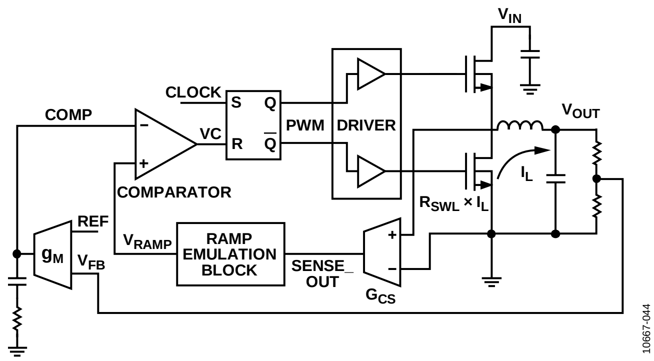

Figure 52. Control Architecture Block Diagram

Pulse Skip Mode

The ADP2442 pulse skip mode is enabled by connecting the SYNC/MODE pin to AGND. In this mode, the pulse skip circuitry turns on during light loads, switching only as necessary to keep the output voltage within regulation. This mode allows the regulator to maintain high efficiency during operation with light loads by reducing switching losses. The pulse skip circuitry includes a comparator, which compares the COMP voltage to a fixed pulse skip threshold.

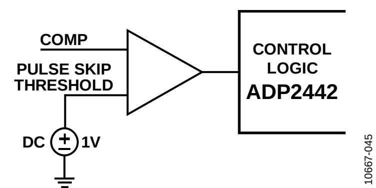

Figure 53. Pulse Skip Comparator

With light loads, the output voltage discharges at a very slow rate (load dependent). When the output voltage is within regulation, the device enters sleep mode and draws a very small quiescent current. As the output voltage drops below the regulation voltage, the COMP voltage rises above the pulse skip threshold. The device wakes up and begins switching until the output voltage is within regulation.

As the load increases, the settling value of the COMP voltage increases. At a particular load, COMP settles above the pulse skip threshold, and the device enters the fixed frequency mode. Therefore, the load current at which COMP exceeds the pulse skip threshold is defined as the pulse skip current threshold; the value varies with the duty cycle and the inductor ripple current.

The measured value of pulse skip threshold over V_{IN} is shown in Figure 19, Figure 20, and Figure 21.

ADJUSTABLE FREQUENCY

The ADP2442 features a programmable oscillator frequency with a resistor connected between the FREQ and AGND pins.

At power-up, the FREQ pin is forced to 1.2 V and current flows from the FREQ pin to AGND; the current value is based on the resistor value on the FREQ pin. Next, the same current replicates in the oscillator to set the switching frequency. Note that the resistor connected to the FREQ pin should be placed as close as possible to the FREQ pin (see the Applications Information section for more information).

POWER GOOD

The PGOOD pin is an open-drain output that indicates the status of the output voltage. When the voltage of the FB pin is between 92% and 109% of the internal reference voltage, the PGOOD output is pulled high, provided there is a pull-up resistor connected to the pin. When the voltage of the FB pin is not within this range, the PGOOD output is pulled low to AGND. The PGOOD threshold is shown in Figure 54.

Likewise, the PGOOD pin is pulled low to AGND when

- The input voltage is below the internal UVLO threshold.
- The EN pin is low.
- A thermal shutdown event has occurred.

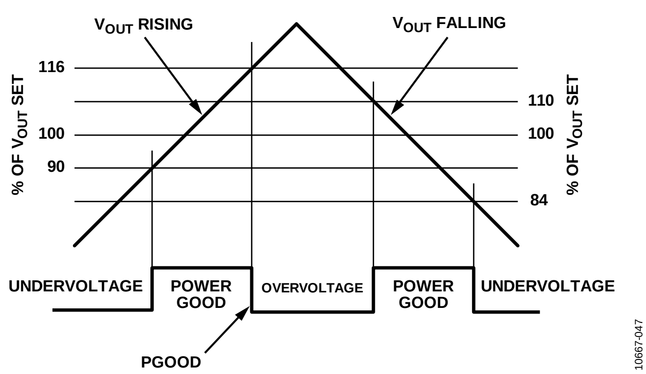

Figure 54. PGOOD Threshold

In a typical application, a pull-up resistor connected between the PGOOD pin and an external supply is used to generate a logic signal. This pull-up resistor should range in value from 30 kΩ to 100 kΩ, and the external supply should be less than 5.5 V.

MODE OF OPERATION

The SYNC/MODE pin is a multifunctional pin. The fixed frequency mode is enabled when SYNC/MODE is connected to VCC or a high logic. When SYNC/MODE is connected to AGND, pulse skip mode is enabled. The external clock can be applied for synchronization.

Table 5. SYNC/MODE Pin Mode of Operation

SYNC/MODE Pin	Mode of Operation
Low	Pulse skip mode
High	Forced fixed frequency mode
Clock Signal	Forced fixed frequency mode

EXTERNAL SYNCHRONIZATION

The external synchronization feature allows the switching frequency of the device to be synchronized to an external clock. The SYNC/MODE input accepts a logic level clock input ranging from 300 kHz to 1 MHz (minimum pulse width = 100 ns) and has high input impedance. For best practices, it is recommended that the set frequency (set by the resistor at the FREQ pin) be within ±30% of the expected clock frequency to ensure stable, reliable, and seamless operation with or without an external SYNC/MODE clock. When the ADP2442 is synchronized to an external clock, the regulator switching frequency is changed to the external clock frequency.

SOFT START

The ADP2442 has an internal soft start feature that allows the output voltage to ramp up in a controlled manner, limiting the inrush current during startup. The ADP2442 internal soft start time is 2 ms.

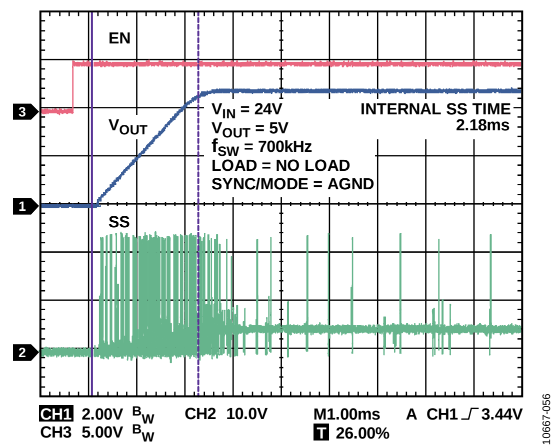

Figure 55. Internal Soft Start

UNDERVOLTAGE LOCKOUT

The undervoltage lockout (UVLO) function prevents the IC from turning on when the input voltage is below the specified operating range to avoid an undesired operating mode. If the input voltage drops below the specified range, the UVLO function shuts off the device. The rising input voltage threshold for the UVLO function is 4.2 V with 200 mV hysteresis. The 200 mV of hysteresis prevents the regulator from turning on and off repeatedly when there is a slow voltage ramp on the VIN pin.

PRECISION ENABLE/SHUTDOWN

The ADP2442 features a precision enable pin (EN) to enable or shutdown the device. The ±5% accuracy lends itself to using a resistor divider from the VIN pin (or another external supply) to program a desired UVLO threshold that is higher than the fixed internal UVLO of 4.2 V. The hysteresis is 100 mV.

If a resistor divider is not used, apply a logic signal instead. A logic high enables the device, and a logic low forces the part into shutdown mode.

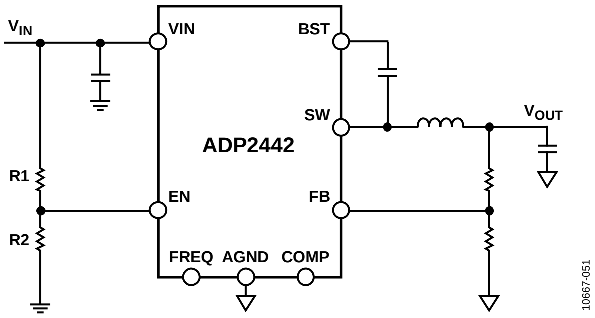

Figure 56. Precision Enable Used as a Programmable UVLO

CURRENT-LIMIT AND SHORT-CIRCUIT PROTECTION

The ADP2442 has a current-limit comparator that compares the current sensed across the low-side power MOSFET to the internally set reference current. If the sensed current exceeds the reference current, the high-side power MOSFET is not turned on in the next cycle and the low-side power MOSFET stays on until the inductor current ramps down below the current-limit level.

If the output is overloaded and the peak inductor current exceeds the preset current limit for more than eight consecutive clock cycles, the hiccup mode current-limit condition occurs. The output goes to sleep for 6 ms, during which time the output is discharged, the average power dissipation is reduced, and the part wakes up with a soft start period. If the current-limit condition is triggered again, the output goes to sleep and wakes up after 6 ms. Figure 37 shows the current-limit hiccup mode when the output is shorted to ground.

THERMAL SHUTDOWN

If the ADP2442 junction temperature rises above 150°C, the thermal shutdown circuit turns off the switching regulator. Extreme junction temperatures can be the result of high current operation, poor circuit board design, or high ambient temperature. A 25°C hysteresis is included so that when a thermal shutdown occurs, the ADP2442 does not return to normal operation until the junction temperature drops below 125°C. Soft start is active upon each restart cycle.

APPLICATIONS INFORMATION

ADIsimPOWER DESIGN TOOL

The ADP2442 is supported by the ADIsimPower design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized to a specific design goal. These tools allow the user to generate a full schematic, bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count while taking into consideration the operating conditions and limitations of the IC and all real external components. The ADIsimPower tool can be found at www.analog.com/adisimpower and the user can request an unpopulated board through the tool.

SELECTING THE OUTPUT VOLTAGE

The output voltage is set using a resistor divider connected between the output voltage and the FB pin (see Figure 57). The resistor divider divides down the output voltage to the 0.6 V FB regulation voltage. The output voltage can be set to as low as 0.6 V and as high as 90% of the power input voltage.

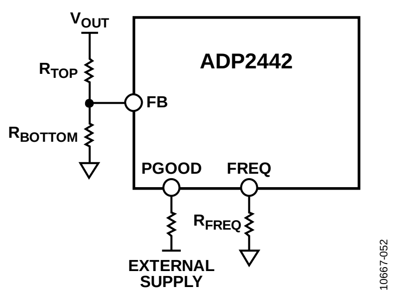

Figure 57. Voltage Divider

The ratio of the resistive voltage divider sets the output voltage, and the absolute value of the resistors sets the divider string current. When calculating the resistor values for lower divider string currents, take into account the small 50 nA (0.1 µA maximum) FB bias current. The FB bias current can be ignored for a higher divider string current; however, using small feedback resistors degrades efficiency at very light loads.

To limit degradation of the output voltage accuracy due to FB bias current to less than 0.005% (0.5% maximum), ensure that the divider string current is greater than 20 µA. To calculate the desired resistor values, first determine the value of the bottom resistor, R_{BOTTOM}, as follows:

$$R_{BOTTOM} = \frac{V_{REF}}{I_{STRING}} \quad (1)$$

where:
V_{REF} is the internal reference and equals 0.6 V.
I_{STRING} is the resistor divider string current.

Next, calculate the value of the top resistor, R_{TOP}, as follows:

$$R_{TOP} = R_{BOTTOM} \times \left(\frac{V_{OUT} - V_{REF}}{V_{REF}}\right) \quad (2)$$

Table 6. Output Voltage Selection

Voltage (V)	R_{TOP} (kΩ)	R_{BOTTOM} (kΩ)
12	190	10
5	73	10
3.3	45	10
1.2	10	10

SETTING THE SWITCHING FREQUENCY

The choice of the switching frequency depends on the required dc-to-dc conversion ratio and is limited by the minimum and maximum controllable duty cycle, as shown in Figure 58. This limitation is due to the requirement of minimum on time and minimum off time for current sensing and robust operation. However, the choice is also influenced by whether there is a need for small external components. For example, higher switching frequencies are required for small, area limited power solutions.

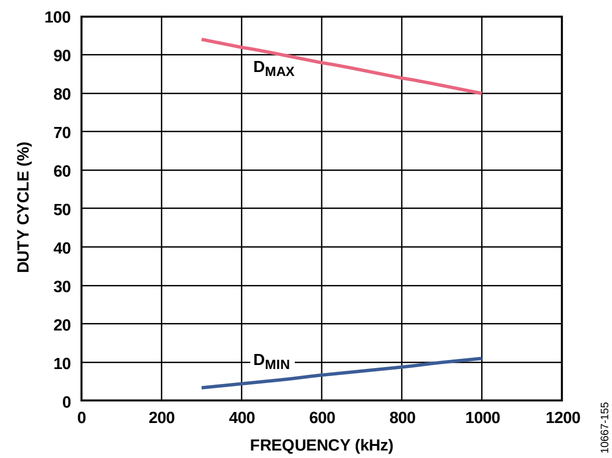

Figure 58. Duty Cycle vs. Switching Frequency

Calculate the value of the frequency resistor by using the following equation:

$$R_{FREQ} = \frac{92{,}500}{f_{SW}} \quad (3)$$

where R_{FREQ} is in kΩ and f_{SW} is in kHz.

Table 7 and Figure 59 provide examples of frequency resistor values that are based on the switching frequency.

Table 7. Frequency Resistor Selection

R_{FREQ}	Frequency
308 kΩ	300 kHz
132 kΩ	700 kHz
92.5 kΩ	1 MHz

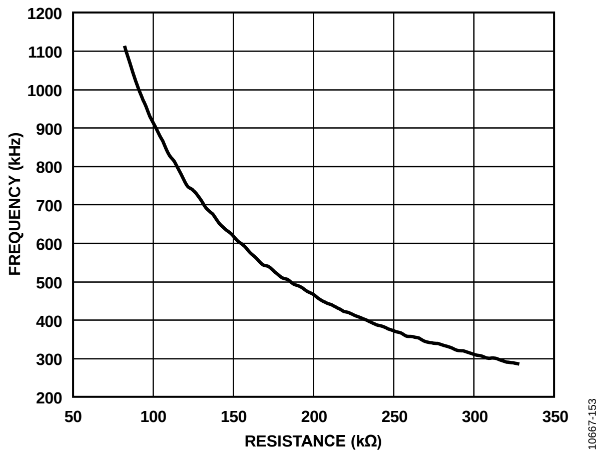

Figure 59. Frequency vs. Resistor

EXTERNAL COMPONENT SELECTION

Input Capacitor Selection

The input current to a buck regulator is pulsating in nature. The current is zero when the high-side switch is off and is approximately equal to the load current when the switch is on. Because switching occurs at reasonably high frequencies (300 kHz to 1 MHz), the input bypass capacitor usually supplies most of the high frequency current (ripple current), allowing the input power source to supply only the average (dc) current. The input capacitor needs a sufficient ripple current rating to handle the input ripple and needs an ESR that is low enough to mitigate the input voltage ripple. In many cases, different types of capacitors are placed in parallel to minimize the effective ESR and ESL.

The minimum input capacitance required for a particular load is

$$C_{IN\_MIN} = \frac{I_{OUT} \times D \times (1 - D)}{(V_{PP} - I_{OUT} \times D \times R_{ESR}) f_{SW}} \quad (4)$$

where:
V_{PP} is the desired input ripple voltage.
R_{ESR} is the equivalent series resistance of the capacitor.
I_{OUT} is the maximum load current.
D is the duty cycle.
f_{SW} is the switching frequency.

For best practice, use a ceramic bypass capacitor because the ESR associated with this type of capacitor is near zero, simplifying the equation to

$$C_{IN\_MIN} = \frac{I_{OUT} \times D \times (1 - D)}{V_{PP} \times f_{SW}} \quad (5)$$

In addition, use a ceramic capacitor with a voltage rating that is 1.5 times the input voltage with X5R and X7R dielectrics. Using Y5V and Z5U dielectrics is not recommended because of their poor temperature and dc bias characteristics. Table 10 shows a list of recommended MLCC capacitors.

For large step load transients, add more bulk capacitance by using electrolytic or polymer capacitors. Ensure that the ripple current rating of the bulk capacitor exceeds the minimum input ripple current of a particular design.

Inductor Selection

The high switching frequency of the ADP2442 allows for minimal output voltage ripple even when small inductors are used. Selecting the size of the inductor involves considering the trade-off between efficiency and transient response. A smaller inductor results in larger inductor current ripple, which provides excellent transient response; however, it degrades efficiency. Because of the high switching frequency of the ADP2442, use shielded ferrite core inductors for their low core losses and low EMI.

The inductor ripple current also affects the stability of the loop because the ADP2442 uses the emulated peak current mode architecture. In the traditional approach of slope compensation, the user sets the inductor ripple current and then sets the slope compensation using an external ramp resistor. In most cases, the inductor ripple current is typically set to be 1/3 of the maximum load current for optimal transient response and efficiency. The ADP2442 has internal slope compensation, which assumes that the inductor ripple current is set to 0.3 A (30% of the maximum load of 1 A), eliminating the need for an external ramp resistor.

For the ADP2442, choose an inductor such that the peak-to-peak ripple current of the inductor is between 0.2 A and 0.5 A for stable operation. Calculate the inductor value as follows:

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \quad (6)$$

$$0.2\ \text{A} \le \Delta I_L \le 0.5\ \text{A}$$

$$\frac{2 \times V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW}} \le L \le \frac{5 \times V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW}}$$

$$L_{IDEAL} = \frac{3.3 \times V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW}} \quad (7)$$

where:
V_{IN} is the input voltage.
V_{OUT} is the desired output voltage.
f_{SW} is the regulator switching frequency.
L is the inductor value.
ΔI_L is the peak-to-peak inductor ripple current.
L_{IDEAL} is the ideal calculated inductor value.

For applications with a wide input (V_{IN}) range, choose the inductor based on the geometric mean ($V_{IN\,(GEOMETRIC)}$) of the input voltage extremes.

$$V_{IN(GEOMETRIC)} = \sqrt{V_{IN\_MAX} \times V_{IN\_MIN}} \quad (8)$$

where:
V_{IN_MAX} is the maximum input voltage.
V_{IN_MIN} is the minimum input voltage.

The inductor value is based on $V_{IN\,(GEOMETRIC)}$ as follows:

$$L_{IDEAL} = \frac{3.3 \times V_{OUT} \times (V_{IN(GEOMETRIC)} - V_{OUT})}{V_{IN(GEOMETRIC)} \times f_{SW}} \quad (9)$$

Table 8. Inductor Values for Various V_{IN}, V_{OUT}, and f_{SW} Combinations

			Inductor Values	
f_{SW} (kHz)	V_{IN} (V)	V_{OUT} (V)	Min (µH)	Max (µH)
300	12	3.3	22	27
300	12	5	27	33
300	24	3.3	27	33
300	24	5	39	47
300	24	12	56	68
300	36	3.3	27	33
300	36	5	39	47
300	36	12	68	82
600	12	3.3	12	15
600	12	5	15	18
600	24	3.3	15	18
600	24	5	18	22
600	24	12	27	33
600	36	3.3	15	18
600	36	5	22	27
1000	12	5	6.8	10
1000	24	5	10	12
1000	24	12	18	22
1000	36	5	12	15

To avoid inductor saturation and ensure proper operation, choose the inductor value so that neither the saturation current nor the maximum temperature rated current ratings are exceeded. Inductor manufacturers specify both of these ratings in data sheets, or the rating can be calculated as follows:

$$I_{L\_PEAK} = I_{LOAD(MAX)} + \frac{\Delta I_L}{2} \quad (10)$$

where:
$I_{LOAD\,(MAX)}$ is the maximum dc load current.
ΔI_L is the peak-to-peak inductor ripple current.
I_{L_PEAK} is the peak inductor current.

Table 9. Recommended Inductors

Value (µH)	Small Inductors (<10 mm × 10 mm)	Large Inductors (>10 mm × 10 mm)
10	XAL4040-103ME	MSS1260
18	LPS6235-183ML	MSS1260
33	LPS6235-33ML	MSS1260
15	XAL4040-153ME	MSS1260

Output Capacitor Selection

The output capacitor selection affects both the output voltage ripple and the loop dynamics of the regulator. The ADP2442 is designed to operate with small ceramic output capacitors that have low ESR and ESL; therefore, the device easily meets tight output voltage ripple specifications. For best performance, use X5R or X7R dielectric capacitors with a voltage rating that is 1.5 times the output voltage and avoid using Y5V and Z5U dielectric capacitors, which have poor temperature and dc bias characteristics. Table 10 lists recommended capacitors from Murata and Taiyo Yuden.

Table 10. Recommended Output Capacitors

	Vendor	
Capacitor	Murata	Taiyo Yuden
10 µF/25 V	GRM32DR71E106KA12L	TMK325B7106KN-TR
22 µF/25 V	GRM32ER71E226KE15L	TMK325B7226MM-TR
47 µF/6.3 V	GCM32ER70J476KE19L	JMK325B7476MM-TR
4.7 µF/50 V	GRM31CR71H475KA12L	UMK325B7475MMT

For acceptable maximum output voltage ripple, determine the minimum output capacitance, $C_{OUT\,(MIN)}$, as follows:

$$\Delta V_{RIPPLE} \cong \Delta I_L \times \left(ESR + \frac{1}{8 \times f_{SW} \times C_{OUT(MIN)}} \right) \quad (11)$$

Therefore,

$$C_{OUT(MIN)} \cong \frac{\Delta I_L}{8 \times f_{SW} \times (\Delta V_{RIPPLE} - \Delta I_L \times ESR)} \quad (12)$$

where:
ΔV_{RIPPLE} is the allowable peak-to-peak output voltage ripple.
ΔI_L is the inductor ripple current.
ESR is the equivalent series resistance of the capacitor.
f_{SW} is the switching frequency of the regulator.

When there is a step load requirement, choose the output capacitor value based on the value of the step load. Use the following equation to determine the maximum acceptable output voltage droop/overshoot caused by the step load:

$$C_{OUT(MIN)} \cong \Delta I_{OUT(STEP)} \times \left(\frac{3}{f_{SW} \times \Delta V_{DROOP}} \right) \quad (13)$$

where:
$\Delta I_{OUT\,(STEP)}$ is the load step.
f_{SW} is the switching frequency of the regulator.
ΔV_{DROOP} is the maximum allowable output voltage droop/overshoot.

Select the larger of the output capacitances derived from Equation 12 and Equation 13. When choosing the type of ceramic capacitor for the output filter of the regulator, select a capacitor with a nominal capacitance that is 20% to 30% larger than the calculated value because the effective capacitance degrades with dc voltage and temperature. Figure 60 shows the capacitance loss resulting from the dc bias voltage for two capacitors (X7R MLCC capacitors from Murata are shown in Figure 60).

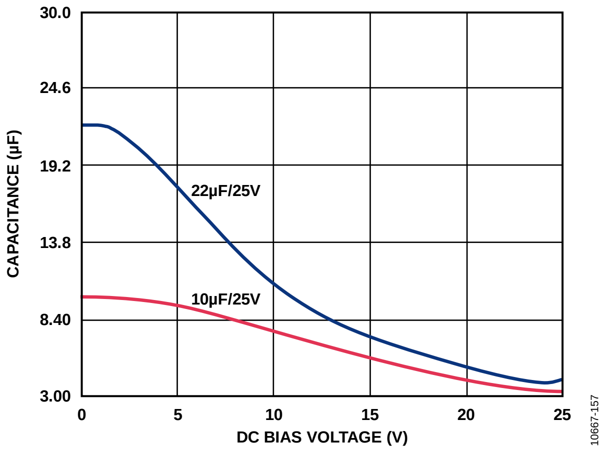

Figure 60. Capacitance vs. DC Voltage

For example, to attain 20 µF of output capacitance with an output voltage of 5 V while providing some margin for temperature variation, use a 22 µF capacitor with a voltage rating of 25 V and a 10 µF capacitor with a voltage rating of 25 V in parallel. This configuration ensures that the output capacitance is sufficient under all conditions and, therefore, that the device exhibits stable behavior.

BOOST CAPACITOR

The boost pin (BST) is used to power up the internal driver for the high-side power MOSFET. In the ADP2442, the high-side power MOSFET is an N-channel device to achieve high efficiency in mid and high duty cycle applications. To power up the high-side driver, a capacitor is required between the BST and SW pins. The size of this boost capacitor is critical because it affects the light load functionality and efficiency of the device. Therefore, choose a boost ceramic capacitor with a value between 10 nF and 22 nF with a voltage rating of 50 V, placing the capacitor as close as possible to the IC. It is recommended to use a boost capacitor within this range because a capacitor beyond 22 nF can cause the LDO to reach the current-limit threshold.

VCC CAPACITOR

The ADP2442 has an internal regulator to power up the internal controller and the low-side driver. The VCC pin is the output of the internal regulator. The internal regulator provides the pulse current when the low-side driver turns on. Therefore, it is recommended that a 1 µF ceramic capacitor be placed between the VCC and PGND pins as close as possible to the IC and that a 1 µF ceramic capacitor be placed between the VCC and AGND pins.

LOOP COMPENSATION

The ADP2442 uses a peak current mode control architecture for excellent load and line transient response. This control architecture has two loops: an inner current loop and an external voltage loop.

The inner current loop senses the current in the low-side switch and controls the duty cycle to maintain the average inductor current. To ensure stable operation when the duty cycle is above 50%, slope compensation is added to the inner current loop.

The external voltage loop senses the output voltage and adjusts the duty cycle to regulate the output voltage to the desired value. A transconductance amplifier with an external series RC network connected to the COMP pin compensates for the external voltage loop, as shown in Figure 61.

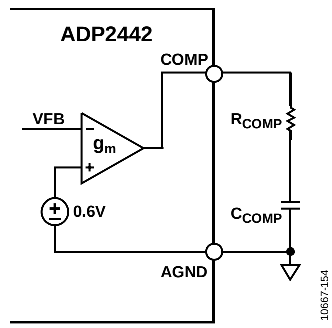

Figure 61. RC Compensation Network

LARGE SIGNAL ANALYSIS OF THE LOOP COMPENSATION

The control loop can be broken down into the following three sections:

- V_{OUT} to V_{COMP}
- V_{COMP} to I_L
- I_L to V_{OUT}

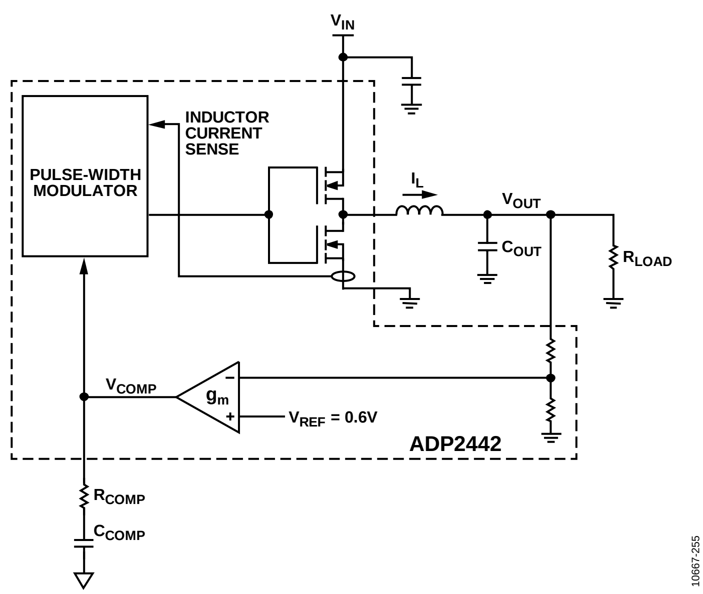

Figure 62. Large Signal Model

Correspondingly, there are three transfer functions:

$$\frac{V_{COMP}(s)}{V_{OUT}(s)} = \frac{V_{REF}}{V_{OUT}} \times g_m \times Z_{COMP}(s) \quad (14)$$

$$\frac{I_L(s)}{V_{COMP}(s)} = G_{CS} \quad (15)$$

$$\frac{V_{OUT}(s)}{I_L(s)} = Z_{FILT}(s) \quad (16)$$

where:
V_{COMP} is the comparator voltage.
I_L is the inductor current.
g_m is the transconductance of the error amplifier and equals 250 µA/V.
G_{CS} is the current sense gain and equals 2 A/V.
V_{OUT} is the output voltage of the regulator.
V_{REF} is the internal reference voltage and equals 0.6 V.
$Z_{COMP}(s)$ is the impedance of the RC compensation network that forms a pole at the origin and a zero, as expressed in Equation 17.

$$Z_{COMP}(s) = \frac{1 + s \times R_{COMP} \times C_{COMP}}{s \times C_{COMP}} \quad (17)$$

$Z_{FILT}(s)$ is the impedance of the output filter and is expressed as

$$Z_{FILT}(s) = \frac{R_{LOAD}}{1 + s \times R_{LOAD} \times C_{OUT}} \quad (18)$$

where s is the angular frequency, which can be written as $s = 2\pi f$.

The overall loop gain, H(s), is obtained by multiplying the three transfer functions previously mentioned as follows:

$$H(s) = g_m \times G_{CS} \times \frac{V_{REF}}{V_{OUT}} \times Z_{COMP}(s) \times Z_{FILT}(s) \quad (19)$$

When the switching frequency (f_{SW}), output voltage (V_{OUT}), output inductor (L), and output capacitor (C_{OUT}) values are selected, the unity crossover frequency can be set to 1/12 of the switching frequency.

At the crossover frequency, the gain of the open-loop transfer function is unity.

$$H(f_{CROSSOVER}) = 1 \quad (20)$$

This yields Equation 21 for the RC compensation network impedance at the crossover frequency.

$$Z_{COMP}(f_{CROSSOVER}) = \frac{2 \times \pi \times f_{CROSSOVER} \times C_{OUT}}{g_m \times G_{CS}} \times \frac{V_{OUT}}{V_{REF}} \quad (21)$$

Placing s = $f_{CROSSOVER}$ in Equation 17,

$$Z_{COMP}(f_{CROSSOVER}) = \frac{1 + 2 \times \pi \times f_{CROSSOVER} \times R_{COMP} \times C_{COMP}}{2 \times \pi \times f_{CROSSOVER} \times C_{COMP}} \quad (22)$$

To ensure that there is sufficient phase margin at the crossover frequency, place the compensator zero at 1/8 of the crossover frequency, as shown in the following equation:

$$f_{ZERO} = \frac{1}{2 \times \pi \times R_{COMP} \times C_{COMP}} \approx \frac{f_{CROSSOVER}}{8} \quad (23)$$

Solving Equation 21, Equation 22, and Equation 23 yields the values for the resistor and capacitor in the RC compensation network, as shown in Equation 24 and Equation 25.

$$R_{COMP} = 0.9 \times \frac{2 \times \pi \times f_{CROSSOVER}}{g_m \times G_{CS}} \times \frac{C_{OUT} \times V_{OUT}}{V_{REF}} \quad (24)$$

$$C_{COMP} = \frac{1}{2 \times \pi \times f_{ZERO} \times R_{COMP}} \quad (25)$$

Using these equations allows calculating the compensations for the voltage loop.

DESIGN EXAMPLE

Consider an application with the following specifications:

- V_{IN}: 24 V ± 10%
- V_{OUT}: 5 V ± 1%
- Switching frequency: 700 kHz
- Load: 800 mA typical
- Maximum load current: 1 A
- Overshoot ≤ 2% under all load transient conditions

CONFIGURATION AND COMPONENTS SELECTION

Resistor Divider

The first step in selecting the external components is to calculate the resistance of the resistor divider that sets the output voltage.

Using Equation 1 and Equation 2,

$$R_{BOTTOM} = \frac{V_{REF}}{I_{STRING}} = \frac{0.6}{60\ \mu A} = 10\ k\Omega$$

$$R_{TOP} = R_{BOTTOM} \times \left(\frac{V_{OUT} - V_{REF}}{V_{REF}} \right)$$

$$R_{TOP} = 10\ k\Omega \times \left(\frac{5\ V - 0.6\ V}{0.6\ V} \right) = 73.3\ k\Omega$$

Switching Frequency

Choosing the switching frequency involves consideration of the trade-off between efficiency and component size. Low frequency improves the efficiency by reducing the gate losses but requires a large inductor. The choice of high frequency is limited by the minimum and maximum duty cycle.

Table 11. Duty Cycle

V_{IN}	Duty Cycle
24 V (Nominal)	$D_{NOMINAL}$ = 20.8%
26 V (10% Above Nominal)	D_{MIN} = 19%
22 V (10% Less than Nominal)	D_{MAX} = 23%

Based on the estimated duty cycle range, choose the switching frequency according to the minimum and maximum duty cycle limitations, as shown in Figure 58. For example, a 700 kHz, frequency is well within the maximum and minimum duty cycle limitations.

Using Equation 3,

$$R_{FREQ} = \frac{92{,}500}{f_{SW}}$$

R_{FREQ} = 132 kΩ

Inductor Selection

Select the inductor by using Equation 7.

$$L_{IDEAL} = \frac{3.3 \times V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW}}$$

$$L_{IDEAL} = \frac{3.3 \times 5\ V \times (24 - 5)\ V}{24\ V \times 700\ kHz} = 18.66\ \mu H \approx 18.3\ \mu H$$

In Equation 7, V_{IN} = 24 V, V_{OUT} = 5 V, $I_{LOAD\ (MAX)}$ = 1 A, and f_{SW} = 700 kHz, which results in L = 18.66 μH. When L = 18 μH (the closest standard value) in Equation 6, ΔI_L = 0.314 A. Although the maximum output current that is required is 1 A, the maximum peak current is 1.6 A. Therefore, the inductor should be rated for higher than 1.6 A current.

Input Capacitor Selection

The input filter consists of a small 0.1 μF ceramic capacitor placed as close as possible to the IC.

The minimum input capacitance required for a particular load is

$$C_{IN\_MIN} = \frac{I_{OUT} \times D \times (1 - D)}{V_{PP} \times f_{SW}}$$

where:
V_{PP} = 50 mV.
I_{OUT} = 1 A.
D = 0.23.
f_{SW} = 700 kHz.

Therefore,

$$C_{IN\_MIN} = \frac{1\ A \times 0.22 \times (1 - 0.22)}{0.05\ V \times 700\ kHz} \approx 4.9\ \mu F$$

Choosing an input capacitor of 10 μF with a voltage rating of 50 V ensures sufficient capacitance over voltage and temperature.

Output Capacitor Selection

Select the output capacitor by using Equation 12 and Equation 13

$$C_{OUT(MIN)} \cong \frac{\Delta I_L}{8 \times f_{SW} \times (\Delta V_{RIPPLE} - \Delta I_L \times ESR)}$$

Equation 12 is based on the output voltage ripple (ΔV_{RIPPLE}), which is 1% of the output voltage.

$$C_{OUT(MIN)} \cong \Delta I_{OUT(STEP)} \left(\frac{3}{f_{SW} \times \Delta V_{DROOP}} \right)$$

Equation 13 calculates the capacitor selection based on the transient load performance requirement of 2%. Perform these calculations, then use the equation that yields the larger capacitor size to select a capacitor.

In this example, the values listed in Table 12 are substituted for the variables in Equation 12 and Equation 13.

Table 12. Requirements

Parameter	Test Conditions/Comments	Value
Ripple Current	Fixed at 0.3 A for the ADP2442	0.3 A
Voltage Ripple	1% of V_{OUT}	50 mV
Voltage Droop Due to Load Transient	2% of V_{OUT}	100 mV
ESR		5 mΩ
f_{SW}		700 kHz

The calculation based on the output voltage ripple (see Equation 12) dictates that the minimum output capacitance is

$$C_{OUT(MIN)} \cong \frac{0.3\ \text{A}}{8 \times 700\ \text{kHz} \times (50\ \text{mV} - 0.3\ \text{A} \times 5\ \text{m}\Omega)} = 1.1\ \mu\text{F}$$

Whereas the calculation based on the transient load (see Equation 13) dictates that the minimum output capacitance is

$$C_{OUT(MIN)} \cong 0.5 \times \frac{3}{700\ \text{kHz} \times 0.1\ \text{V}} \approx 22\ \mu\text{F}$$

To meet both requirements, use the value determined by the latter equation. As shown in Figure 60, capacitance degrades with dc bias; therefore, choose a capacitor that is 1.5 times the calculated value.

$$C_{OUT} = 1.5 \times 22\ \mu\text{F} = 32\ \mu\text{F}$$

Compensation Selection

Calculate the compensation component values for the feedback loop using the following equations:

$$R_{COMP} = 0.9 \times \frac{2 \times \pi \times f_{CROSSOVER}}{g_m \times G_{CS}} \times \frac{C_{OUT} \times V_{OUT}}{V_{REF}}$$

$$C_{COMP} = \frac{1}{2 \times \pi \times f_{ZERO} \times R_{COMP}}$$

Selecting the crossover frequency to be 1/12 of the switching frequency and placing the zero frequency at 1/8 of the crossover frequency ensures that there is adequate phase margin in the system.

Table 13. Calculated Parameter Value

Parameter	Test Conditions/Comments	Value
$f_{CROSSOVER}$	1/12 of f_{SW}	58.3 kHz
f_{ZERO}	1/8 of $f_{CROSSOVER}$	7.3 kHz
V_{REF}	Fixed reference	0.6 V
g_m	Transconductance of error amplifier	250 µA/V
G_{CS}	Current sense gain	2 A/V
C_{OUT}	Output capacitor	22 µF
V_{OUT}	Output voltage	5 V

Based on the values listed in Table 13, calculate the compensation value:

$$R_{COMP} = 0.9 \times \frac{2 \times \pi \times 58.3}{250 \times 2} \times \frac{22 \times 5}{0.6} \approx 121\ \text{k}\Omega$$

The closest standard resistor value is 118 kΩ. Therefore,

$$C_{COMP} = \frac{1}{2 \times \pi \times 7.3 \times 118} = 185\ \text{pF} \approx 180\ \text{pF}$$

SYSTEM CONFIGURATION

Configure the system as follows; though the steps are not sequential, they all must be completed:

- Connect a capacitor of 1 µF between the VCC and PGND pins and another capacitor of 1 µF between the VCC and AGND pins. For best performance, use ceramic X5R or X7R capacitors with a 25 V voltage rating.
- Connect a ceramic capacitor of 10 nF with a 50 V voltage rating between the BST and SW pins.
- Connect a resistor between the FREQ and AGND pins as close as possible to the IC.
- If using the power-good feature, connect a 50 kΩ pull-up resistor to a 5 V external supply.
- For synchronization, connect an external clock with a frequency of 700 kHz to the SYNC/MODE pin. Connect the external clock to AGND to activate pulse skip mode or connect it to VCC for forced fixed frequency mode.

See Figure 63 for a schematic of this design example and Table 14 for the calculated component values.

TYPICAL APPLICATION CIRCUITS

DESIGN EXAMPLE

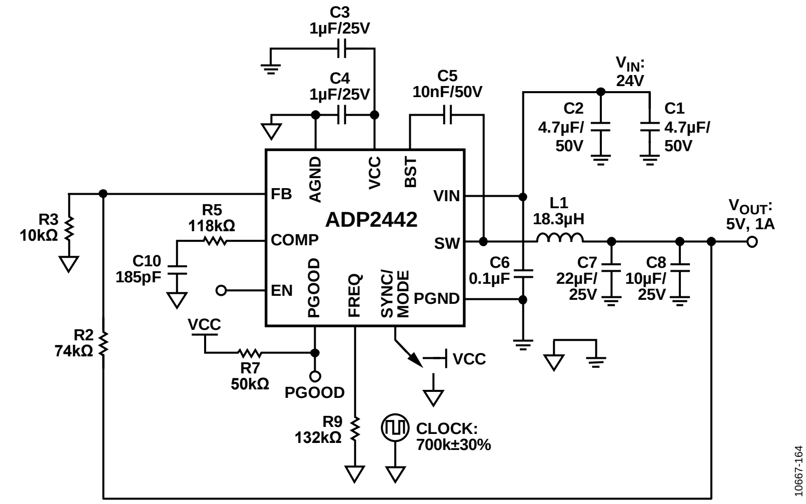

Figure 63. Typical Application Circuit, V_{IN} = 24 V ± 10%, V_{OUT} = 5 V, f_{SW} = 700 kHz

Table 14. Calculated Component Values for Figure 63

Quantity	Reference	Value	Description	Part Number
2	C1, C2	4.7 µF	Capacitor ceramic, X7R, 50 V	GRM31CR71H475KA12L
2	C3, C4	1 µF	Capacitor ceramic, 1 µF, 25 V, X7R, 10%, 0603	GRM188R71E105KA12D
2	C5	10 nF	Capacitor ceramic, 10 nF, 50 V, 10%, X7R, 603	ECJ-1VB1H103K
1	C7	22 µF	Capacitor ceramic, 22 µF, 25 V, X7R, 1210	GRM32ER71E226K
1	C8	10 µF	Capacitor ceramic, 10 µF, 25 V, X7R, 1210	GRM32DR71E106KA12L
1	L1	18.3 µH	Inductor	CoilCraft MSS1260T-183NLB
1	C6	0.1 µF	Capacitor ceramic, 0.1 µF, 50 V, X7R, 0805	ECJ-2FB1H104K
1	C10	185 pF	Capacitor ceramic, 50 V	Determined by user
1	R9	132 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user
1	R5	118 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user
1	R2	74 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user
2	R3	10 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user
1	R7	50 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user

OTHER TYPICAL CIRCUIT CONFIGURATIONS

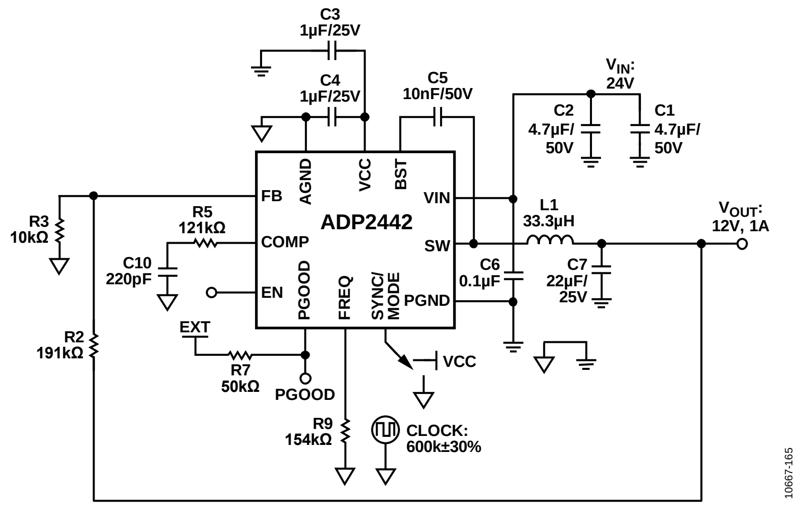

Figure 64. Typical Application Circuit, V_{IN} = 24 V ± 10%, V_{OUT} = 12 V, f_{SW} = 600 kHz

Table 15. Calculated Component Values for Figure 64

Quantity	Reference	Value	Description	Part Number
2	C1, C2	4.7 µF	Capacitor ceramic, X7R, 50 V	GRM31CR71H475KA12L
2	C3, C4	1 µF	Capacitor ceramic, 1 µF, 25 V, X7R, 10%, 0603	GRM188R71E105KA12D
2	C5	10 nF	Capacitor ceramic, 10000 pF, 50 V, 10%, X7R, 0603	ECJ-1VB1H103K
1	C7	22 µF	Capacitor ceramic, 22 µF, 25 V, X7R, 1210	GRM32ER71E226K
1	C8	N/A[1]	N/A[1]	N/A[1]
1	L1	33.3 µH	Inductor	CoilCraft MSS1038-333ML
1	C6	0.1 µF	Capacitor ceramic, 0.1 µF, 50 V, X7R, 0805	ECJ-2FB1H104K
1	C10	220 pF	Capacitor ceramic, 50 V	Determined by user
1	R9	154 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user
1	R5	121 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user
1	R2	191 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user
2	R3	10 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user
1	R7	50 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user

[1] N/A means not applicable.

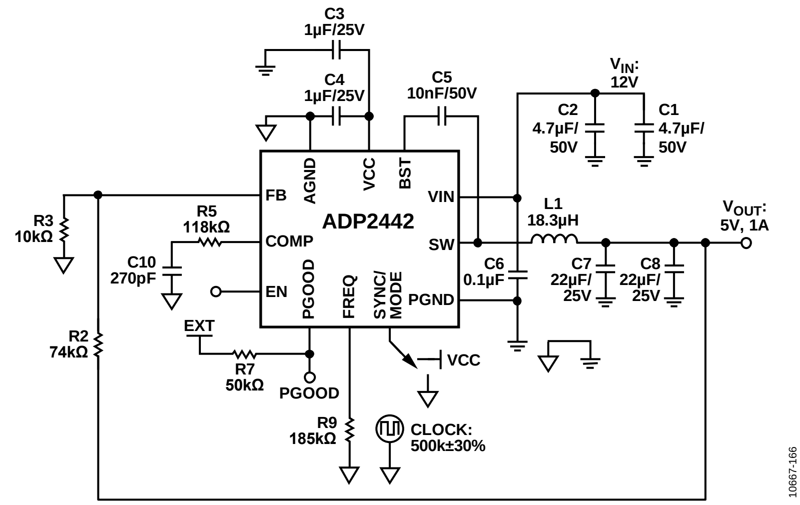

Figure 65. Typical Application Circuit, V_{IN} = 12 V ± 10%, V_{OUT} = 5 V, f_{SW} = 500 kHz

Table 16. Calculated Component Values for Figure 65

Quantity	Reference	Value	Description	Part Number
2	C1, C2	4.7 µF	Capacitor ceramic, X7R, 50 V	GRM31CR71H475KA12L
2	C3, C4	1 µF	Capacitor ceramic, 1 µF, 25 V, X7R, 10%, 0603	GRM188R71E105KA12D
2	C5	10 nF	Capacitor ceramic, 10 nF, 50 V, 10%, X7R, 0603	ECJ-1VB1H103K
1	C7	22 µF	Capacitor ceramic, 22 µF, 25 V, X7R, 1210	GRM32ER71E226K
1	C8	22 µF	Capacitor ceramic, 22 µF, 25 V, X7R, 1210	Determined by user
1	L1	18.3 µH	Inductor	CoilCraft MSS1038-183ML
1	C6	0.1 µF	Capacitor ceramic, 0.1 µF, 50 V, X7R, 0805	ECJ-2FB1H104K
1	C10	270 pF	Capacitor ceramic, 50 V	Determined by user
1	R9	185 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user
1	R5	118 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user
1	R2	74 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user
1	R3	10 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user
1	R7	50 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user

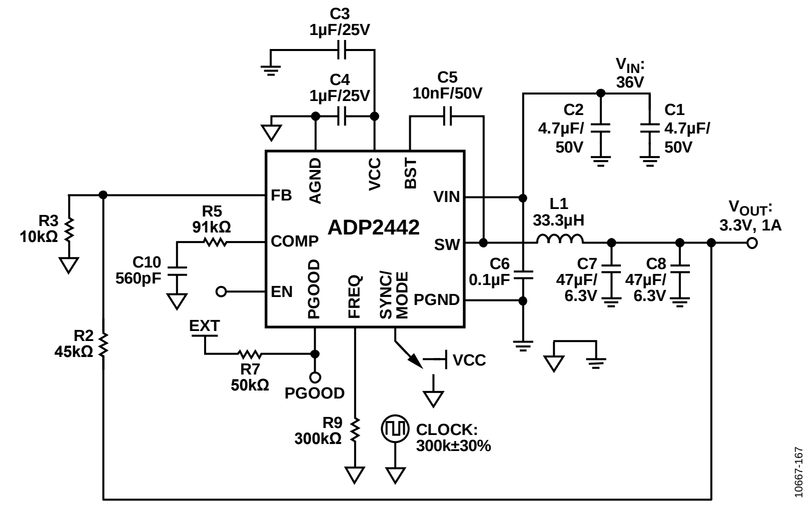

Figure 66. Typical Application Circuit, V_{IN} = 36 V ± 10%, V_{OUT} = 3.3 V, f_{SW} = 300 kHz

Table 17. Calculated Component Values for Figure 66

Quantity	Reference	Value	Description	Part Number
2	C1, C2	4.7 µF	Capacitor ceramic, X7R, 50 V	GRM31CR71H475KA12L
2	C3, C4	1 µF	Capacitor ceramic, 1 µF, 25 V, X7R, 10%, 0603	GRM188R71E105KA12D
2	C5	10 nF	Capacitor ceramic, 10 nF, 50 V, 10%, X7R, 0603	ECJ-1VB1H103K
1	C7	47 µF	Capacitor ceramic, 47 µF, 6.3 V, X7R, 1210	GRM32ER70J476KE20L
1	C8	47 µF	Capacitor ceramic, 47 µF, 6.3 V, X7R, 1210	GRM32ER70J476KE20L
1	L1	33.3 µH	Inductor	CoilCraft MSS1038T-333ML
1	C6	0.1 µF	Capacitor ceramic, 0.1 µF, 50 V, X7R, 0805	ECJ-2FB1H104K
1	C10	560 pF	Capacitor ceramic, 50 V	Determined by user
1	R9	300 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user
1	R5	91 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user
1	R2	45 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user
1	R3	10 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user
1	R7	50 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user

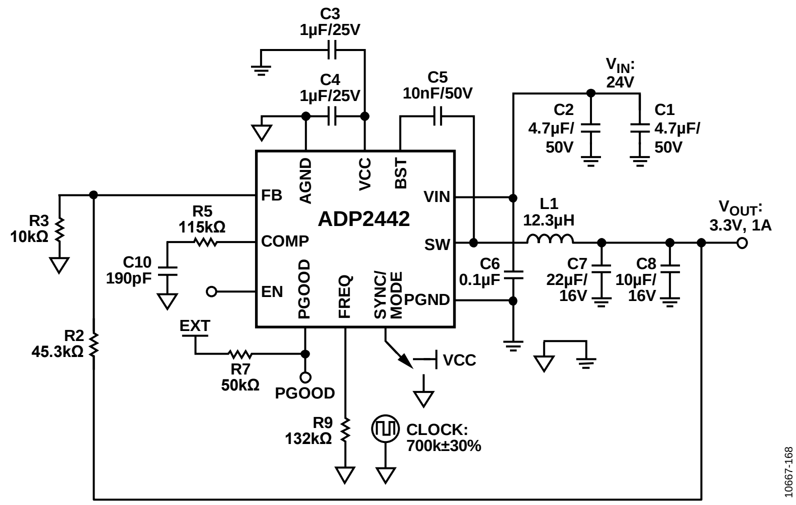

Figure 67. Typical Application Circuit, V_{IN} = 24 V ± 10%, V_{OUT} = 3.3 V, f_{SW} = 700 kHz

Table 18. Calculated Component Values for Figure 67

Quantity	Reference	Value	Description	Part Number
2	C1, C2	4.7 µF	Capacitor ceramic, X7R, 50 V	GRM31CR71H475KA12L
2	C3, C4	1 µF	Capacitor ceramic, 1 µF, 25 V, X7R, 10%, 0603	GRM188R71E105KA12D
2	C5	10 nF	Capacitor ceramic, 10 nF, 50 V, 10%, X7R, 0603	ECJ-1VB1H103K
1	C7	22 µF	Capacitor ceramic, 22 µF, 16 V, X7R, 1210	GRM32ER71C226KEA8L
1	C8	10 µF	Capacitor ceramic, 10 µF, 25 V, X7R, 1210	GRM32DR71E106KA12L
1	L1	12.3 µH	Inductor	CoilCraft MSS1038T-123ML
1	C6	0.1 µF	Capacitor ceramic, 0.1 µF, 50 V, X7R, 0805	ECJ-2FB1H104K
1	C10	190 pF	Capacitor ceramic, 50 V	Determined by user
1	R9	132 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user
1	R5	115 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user
1	R2	45.3 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user
1	R3	10 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user
1	R7	50 kΩ	Resistor, 1/10 W, 1%, 0603, SMD	Determined by user

POWER DISSIPATION AND THERMAL CONSIDERATIONS

POWER DISSIPATION

The efficiency of a dc-to-dc regulator is

$$Efficiency = \frac{P_{OUT}}{P_{IN}} \times 100\% \quad (26)$$

where:
P_{IN} is the input power.
P_{OUT} is the output power.

The power loss of a dc-to-dc regulator is

$$P_{LOSS} = P_{IN} - P_{OUT}$$

There are four main sources of power loss in a dc-to-dc regulator

- Inductor losses
- Power switch conduction losses
- Switching losses
- Transition losses

Inductor Losses

Inductor conduction losses are caused by the flow of current through the inductor DCR (internal resistance). The inductor power loss (excluding core loss) is

$$P_L = I_{OUT}^2 \times DCR_L \quad (27)$$

Power Switch Conduction Losses

Power switch conduction losses are caused by the output current, I_{OUT}, flowing through the N-channel MOSFET power switches that have internal resistance, $R_{DS(ON)}$. The amount of power loss can be approximated as follows:

$$P_{COND} = [R_{DS(ON)-HIGH\ SIDE} \times D + R_{DS(ON)-\ LOW\ SIDE} \times (1 - D)] \times I_{OUT}^2 \quad (28)$$

Switching Losses

Switching losses are associated with the current drawn by the driver to turn the power devices on and off at the switching frequency. Each time a power device gate is turned on and off, the driver transfers a charge (ΔQ) from the input supply to the gate and then from the gate to ground.

The amount of switching loss can by calculated as follows:

$$P_{SW} = Q_{G\_TOTAL} \times V_{IN} \times f_{SW} \quad (29)$$

where:
Q_{G_TOTAL} is the total gate charge of both the high-side and low-side devices and is approximately 18 nC.
f_{SW} is the switching frequency.

Transition Losses

Transition losses occur because the N-channel MOSFET power switch cannot turn on or off instantaneously. During a switch node transition, the power switch provides all of the inductor current, and the source-to-drain voltage of the power switch is half the input, resulting in power loss. Transition losses increase as the load current and input voltage increase; these losses occur twice for each switching cycle.

The transition losses can be calculated as follows:

$$P_{TRANS} = \frac{V_{IN}}{2} \times I_{OUT} \times (t_{ON} + t_{OFF}) f_{SW} \quad (30)$$

where t_{ON} and t_{OFF} are the rise time and fall time of the switch node and are each approximately 10 ns for a 24 V input.

THERMAL CONSIDERATIONS

The power dissipated by the regulator increases the die junction temperature, T_J, above the ambient temperature, T_A, as follows:

$$T_J = T_A + T_R \quad (31)$$

where the temperature rise, T_R, is proportional to the power dissipation, P_D, in the package.

The proportionality coefficient is defined as the thermal resistance from the junction temperature of the die to the ambient temperature, as follows:

$$T_R = \theta_{JA} + P_D \quad (32)$$

where θ_{JA} is the junction-to-ambient thermal resistance and equals 40°C/W for the JEDEC board (see Table 3).

When designing an application for a particular ambient temperature range, calculate the expected ADP2442 power dissipation (P_D) due to the conduction, switching, and transition losses using Equation 28, Equation 29, and Equation 30, and then estimate the temperature rise using Equation 31 and Equation 32. Improved thermal performance can be achieved by good board layout.

For example, on the ADP2442 evaluation board (ADP2442-EVALZ), the measured θ_{JA} is <30°C/W. Thermal performance of the ADP2442-EVALZ evaluation board is shown in Figure 68 and Figure 69.

EVALUATION BOARD THERMAL PERFORMANCE

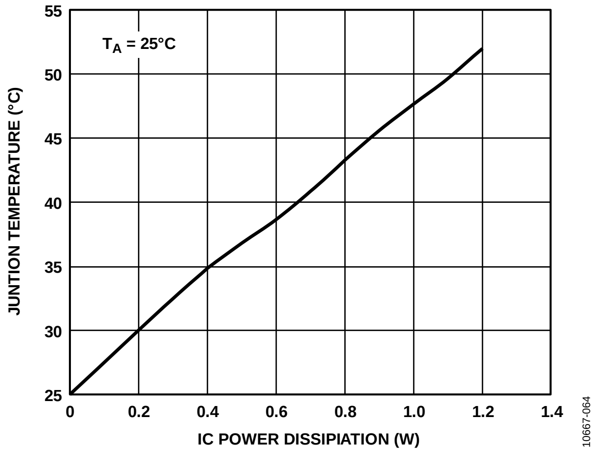

Figure 68. Junction Temperature vs. Power Dissipation Based on ADP2442-EVALZ

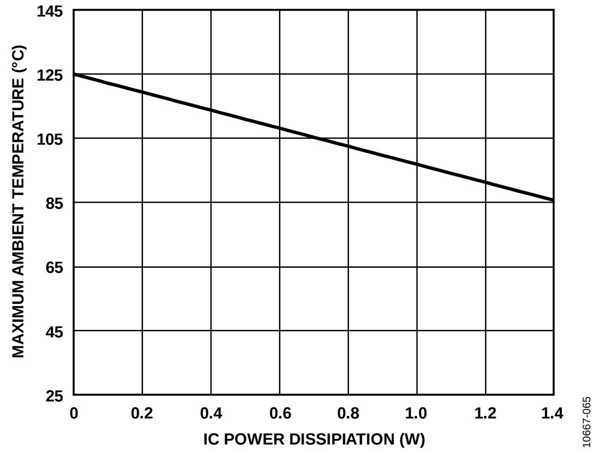

Figure 69. Maximum Ambient Temperature vs. Power Dissipation Based on ADP2442-EVALZ

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Good printed circuit board (PCB) layout is essential for obtaining optimum performance. Poor PCB layout degrades the output voltage ripple; the load, line, and feedback regulation; and the EMI and electromagnetic compatibility performance. For optimum layout, refer to the following guidelines:

- Use separate analog and power ground planes. Connect the ground reference of sensitive analog circuitry, such as the output voltage divider component and the compensation and frequency resistor, to analog ground. In addition, connect the ground references of power components, such as input and output capacitors, to power ground. Connect both ground planes to the exposed pad of the ADP2442.
- Place one end of the input capacitor as close as possible to the VIN pin, and connect the other end to the closest power ground plane.
- Place a high frequency filter capacitor between the VIN and PGND pins, as close as possible to the PGND pin.
- VCC is the internal regulator output. Place a 1 μF capacitor between the VCC and AGND pins and another 1 μF capacitor between the VCC and PGND pins. Place the capacitors as close as possible to the pins.
- Ensure that the high current loop traces are as short and wide as possible. Make the high current path from C_{IN} through L, C_{OUT}, and the power ground plane back to C_{IN} as short as possible. To accomplish this, ensure that the input and output capacitors share a common power ground plane.
- Make the high current path from the PGND pin through L and C_{OUT} back to the power ground plane as short as possible. To do this, ensure that the PGND pin is tied to the PGND plane as close as possible to the input and output capacitors (see Figure 70).
- Connect the ADP2442 exposed pad to a large copper plane to maximize its power dissipation capability.
- Place the feedback resistor divider network as close as possible to the FB pin to prevent noise pickup. Keep the length of the trace connecting the top of the feedback resistor divider to the output as short as possible and, to avoid noise pickup, also keep it away from the high current traces and switch node. Place an analog ground plane on either side of the FB trace to further reduce noise pickup.
- The placement and routing of the compensation components are critical for optimum performance of ADP2442. Place the compensation components as close as possible to the COMP pin. Use 0402 sized compensation components to allow closer placement, which in turn reduces parasitic noise.
- Surround the compensation components with AGND to prevent noise pickup.
- The FREQ pin is sensitive to noise; therefore, place the frequency resistor as close as possible to the FREQ pin and route it with minimal trace length.
- Ground the small signal components to the analog ground path.

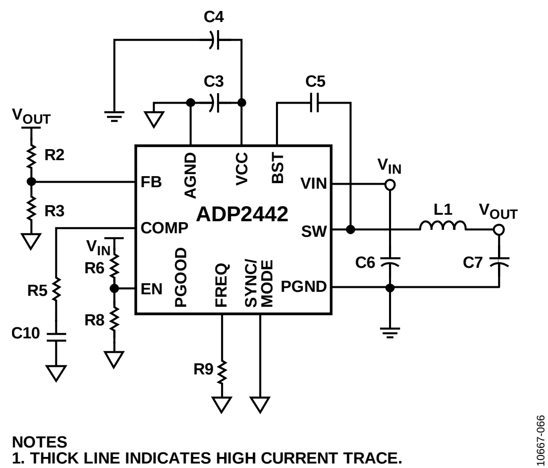

Figure 70. High Current Trace

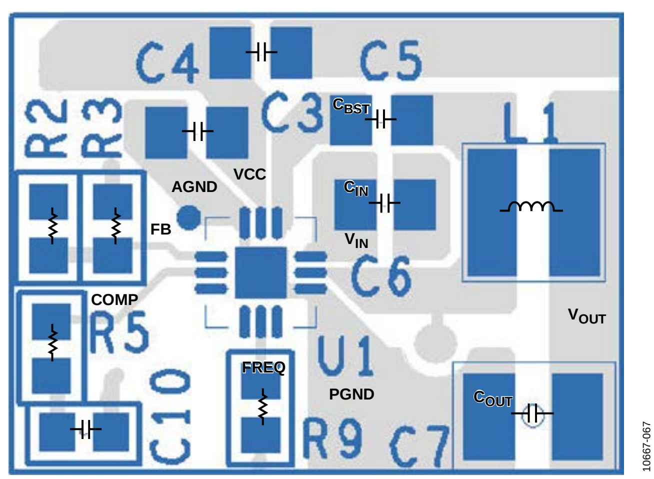

Figure 71. PCB Top Layer Placement

OUTLINE DIMENSIONS

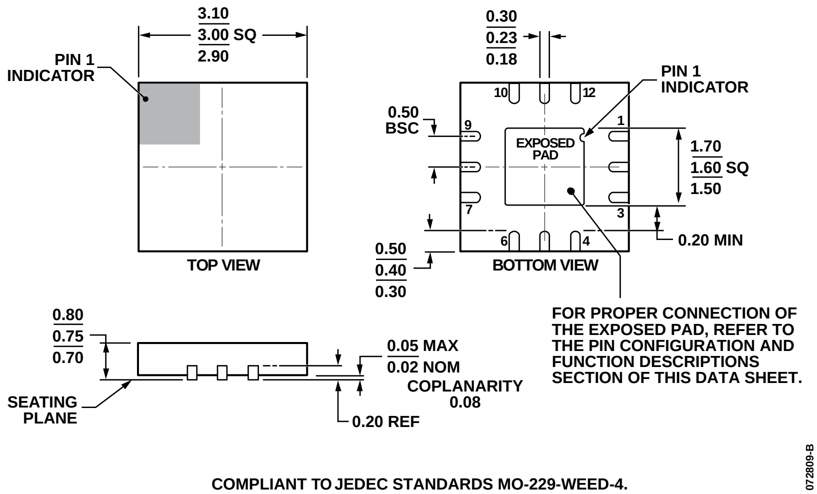

Figure 72. 12-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm × 3 mm Body, Very Very Thin Quad
(CP-12-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Output Voltage	Temperature Range	Package Description	Package Option	Branding Code
ADP2442ACPZ-R7	Adjustable	−40°C to +125°C	12-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-12-6	LK5
ADP2442-EVALZ			Evaluation Board (Preset to 5 V)		

[1] Z = RoHS Compliant Part.

NOTES

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